Shark Bay Platform

PCB Version	SA
Project name	Great Bear
Project Code	NA
PCB Number	13040
PCB Size	244mmX 244mm, t=1.6mm, 4-layers
PCB P/N	(1)48.3EQ14.0SA (2)48.3EQ17.0SA
SCH Ver	X00

On Board Header and Jump setting

CONN	Default	DESCRIPTION
MECLR1	1-X	FOR AUD_LINK_SDO_R ENABLE AND FLASH
CMCLR1	1-3	Reset CMOS data (Debug Only)
PWCLR1	1-3	PASSWORD CLEAR
USBF3		2X10 pin USB3.0 header
USBF1		2X5 pin USB2.0 header
AUDF1		2X5 Front Panel Audio header
FNCPU1		1X4 pin CPU FAN
ATX1		2X12 ATX POWER CONN
XDPC1		60 pin XDP connector for CPU
LPC1		2X7 LPC debug port header (Debug Only)
LEDH1		2X6 Front Panel Header

Board ID

[4..1]	Description
1110	

Major IC version/part number/vender

FUNCTION	Description	Version	WST P/N	Vendor
PCH		C2		INTEL
Realtek Lan	IC LAN RTL8151GD-CG QFN 32P(DELL)		71.08151.M06	REALTEK
SIO	IC SUPER IO IT8772E/EX LQFP 64P		71.08772.B0G	ITE
Audio Codec	IC AUDIO CODEC ALC3600-CG LQFP 48P		71.03600.00G	REALTEK

Index

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	POWER Map	
08	GPIO TABLE	
09	TBD	
10	CPU uLGA 1150_1	
11	CPU uLGA 1150_2	
12	CPU uLGA 1150_3	
13	CPU uLGA 1150_4	
14	XDP/80 PORT HEADER	
15	DDR3 CHA DIMM 0	
16	TBD	
17	DDR3 CHB DIMM 0	
18	TBD	
19	Lynxpoint_AUDIO/GPIO/SPI	
20	Lynxpoint_CLK	
21	Lynxpoint_SATA/FAN/DP/VGA	
22	Lynxpoint_FDI/PCIE/DMI/USB	
23	Lynxpoint_GND/STRAPS	
24	Lynxpoint_POWER	
25	SATA Port	
26	PCIEX16 CONNECTOR	
27	VGA Port	
28	HDMI Port	
29	Display Port (TBD)	
30	FRONT USB3.0 HEADER	
31	USB+RJ45	
32	TBD	
33	REAR USB3.0	
34	USB2.0	
35	LAN RTL8151GD	
36	AUDIO_ALC3600	
37	AUDIO CODEC JACKS	
38	PCIE to PCI BRIDGE_IT8893E	
39	SIO_ITE8772	
40	FAN CIRCUITS/HOLE	
41	TPM(NEW)	
42	PCIEX1 CONNECTOR	
43	MINI PCIE SLOT	
44	PCI SLOT	
45	PWR/FNT PNL	
46	DUAL POWER	
47	DDR POWER	
48	SYSTEM POWER	
49	TBD	
50	CPU_VRD 12-5_1	
51	CPU_VRD 12-5_2	

BOM Configuration
Unmount: (R)
Debug: (P)
SPI Socket: (X)
General: (G)
Great Bear: (B)

<Variant Name>

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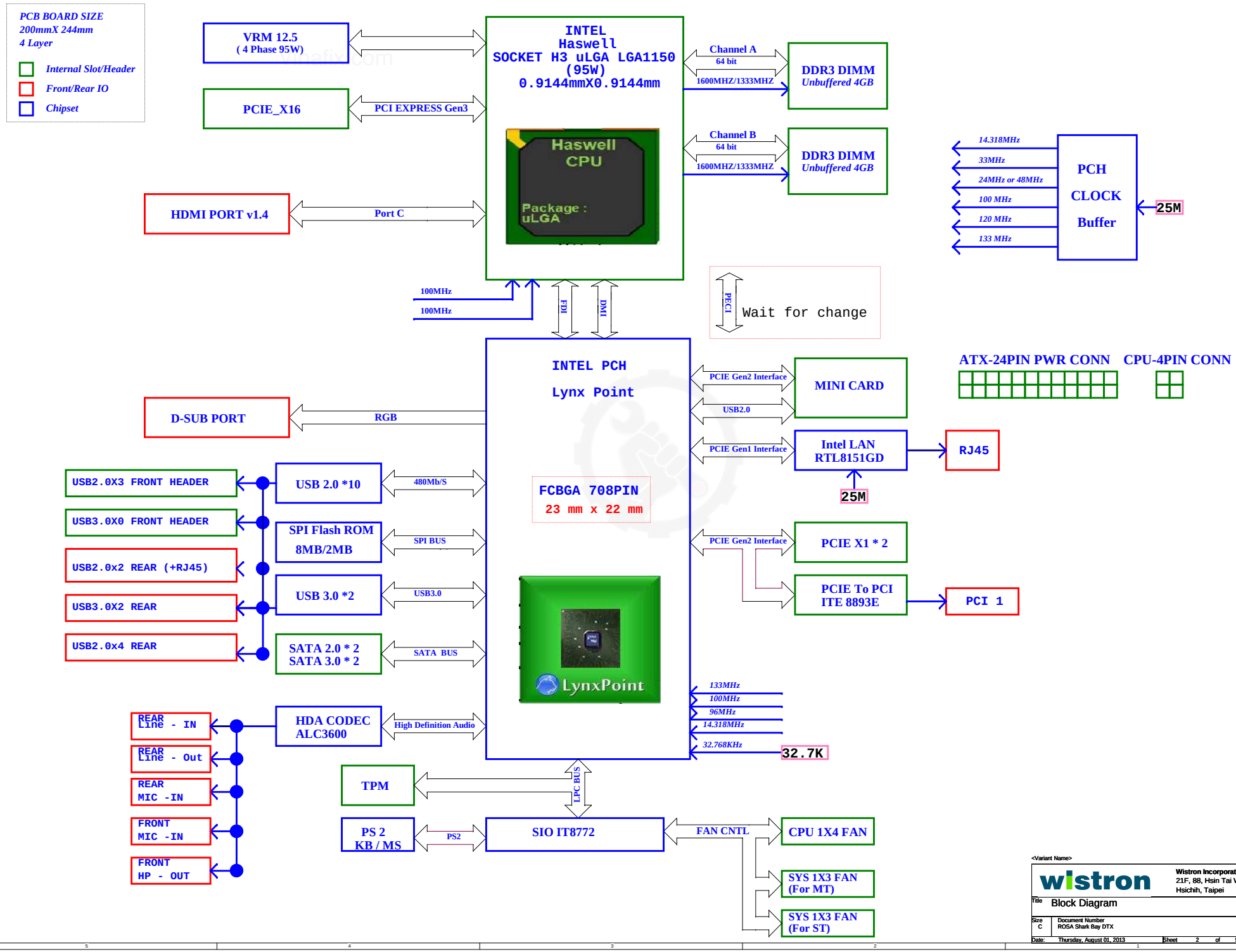
Title: Cover Page

Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Thursday, August 01, 2013 | Sheet 1 of 52



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Title: Block Diagram

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 2 of 52

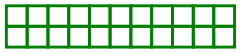
CPU 2X2 POWER CONN

VCC12CPU
Peak 18A
Continue 14A

→ PWM: NCP81102, NCP81161*3 | SIR172DP*6, SIRA12DP*6 → V_CPU_CORE: TDC=85A, Imax=112A

3 Phase Design

ATX 2X12 POWER CONN



SB3V → COMP: LM358 | N-MOSFET: AO4468 → V_1P05_PCH: TDC=6.2A, Imax=6.2A

+12V 10 A
VCC 14 A
VCC5A 1A
VCC3 19 A
-12V 0.2A

1 Phase Design

SWITCH: N-MOSFET, P-MOSFET → 5V_DUAL: TDC= ?A, Imax= 13.3A → PWM: RT8237AZQW | SIR172ADP*1, SIRA12DP*1 → V_SM: 2 channel, TDC=?A, Imax=25A → LDO: RT8237 → V_SM_VTT: TDC=1.1A, Imax=1.1A

SWITCH: N-MOSFET, P-MOSFET → 5VDUAL_USB_R: TDC= ?A, Imax=1A+3.6A

BATTERY → DIODE: BAS40C → V_3P0_BAT_VERG: TDC=6 uA, Imax=6 uA

SWITCH: N-MOSFET, P-MOSFET → 5VDUAL_USB_F: TDC= ?A, Imax= 1+1.8A

P-MOSFET: DMP2130L-7 → SB5V: TDC= ?A, Imax= 1.5A → PWM: RT8015AGQW → V_1P05_ME: TDC=?A, Imax=1A

SWITCH: P-MOSFET → V_3P3_EPW: TDC= ?A, Imax= 0.016A

LDO: APL1085 → V_3P3_A: TDC= 1.5A, Imax= 6A

P-MOSFET: DMP2130L-7 → SB3V: TDC= 1.5A, Imax= 1.5A

SWITCH: N-MOSFET, P-MOSFET → V_3P3_PCIVAUX: TDC= ?A, Imax= 1.5A

LDO: APL5930 → V_1P5_PCH: TDC=?A, Imax=0.35A → V_1P5_DAC_FB: TDC=?A, Imax=0.1A

SWITCH: N-MOSFET, P-MOSFET → V_3P3_LAN: TDC= ?A, Imax= 0.218A

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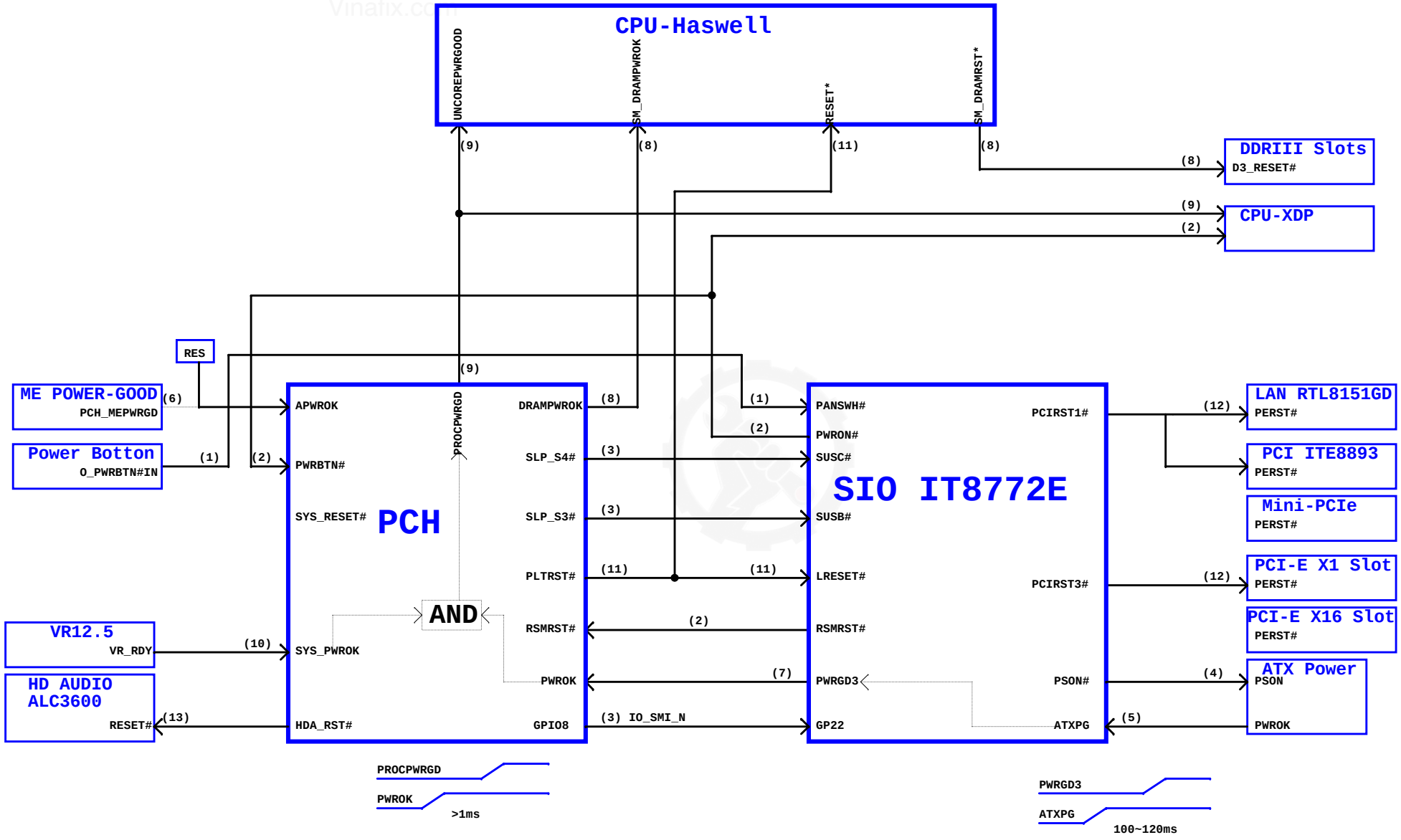
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 3 of 52

RESET / Power Good MAP



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Title: RESET / Power Good MAP

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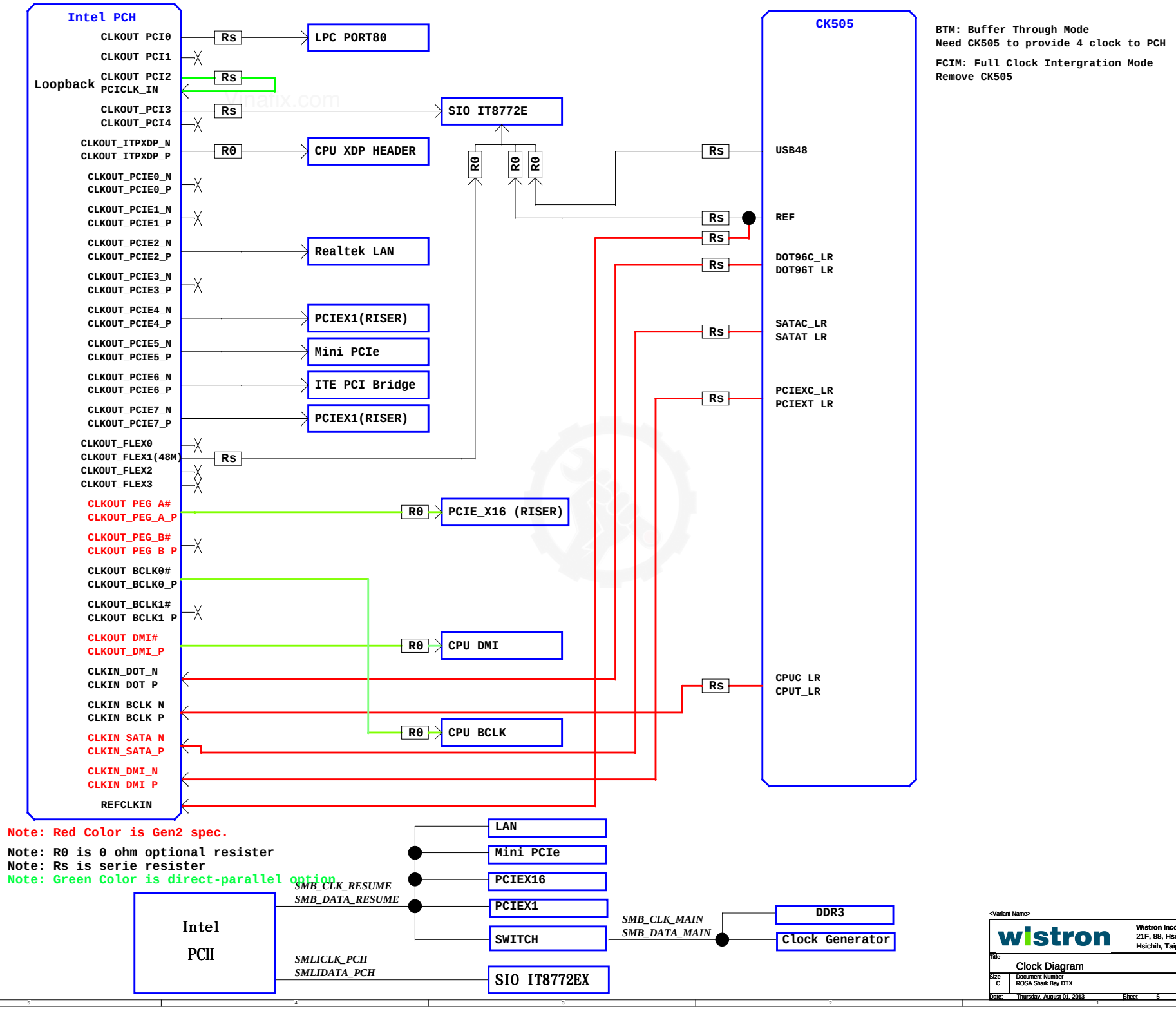
Date: Thursday, August 01, 2013 Sheet 4 of 52



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Title: Clock Diagram

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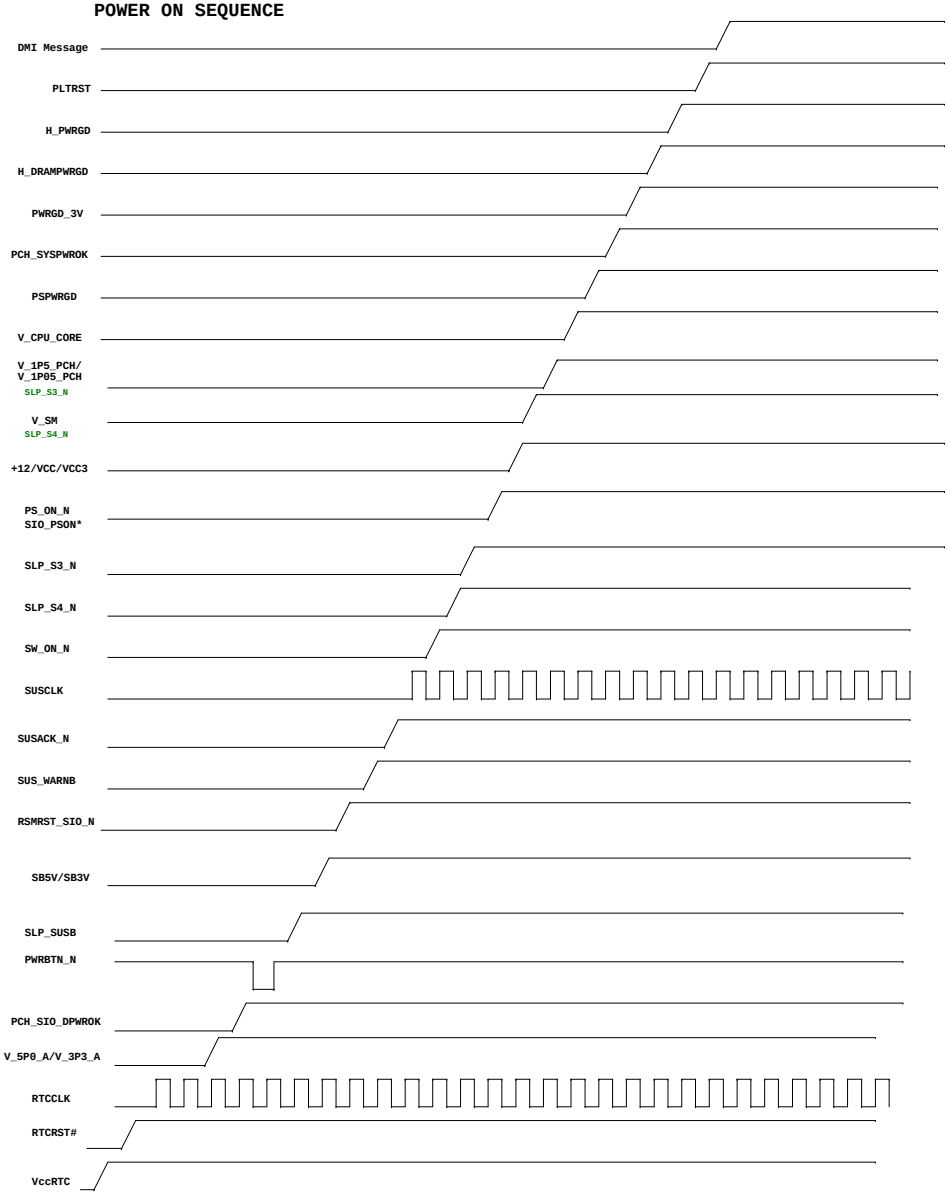
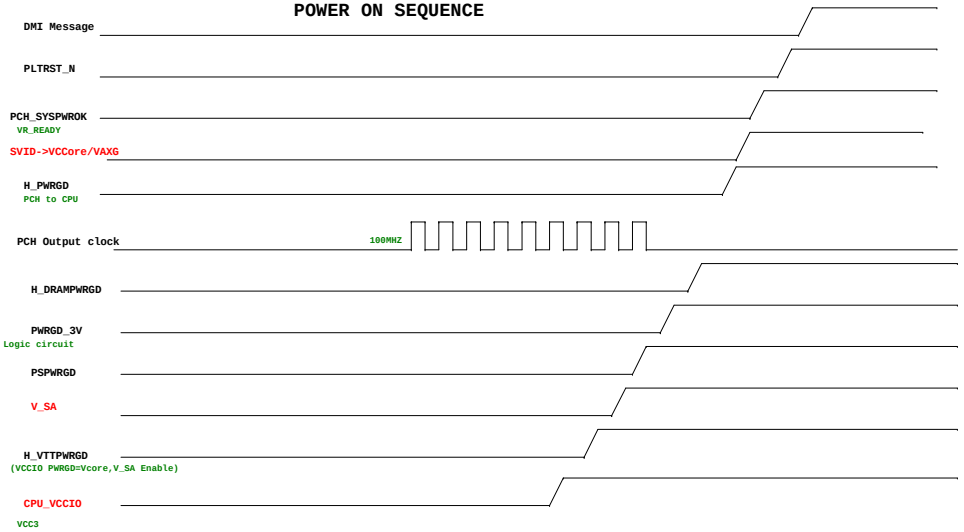
Date: Thursday, August 01, 2013 Sheet 5 of 52

POWER ON SEQUENCE



POWER ON SEQUENCE



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Title: Power Sequence

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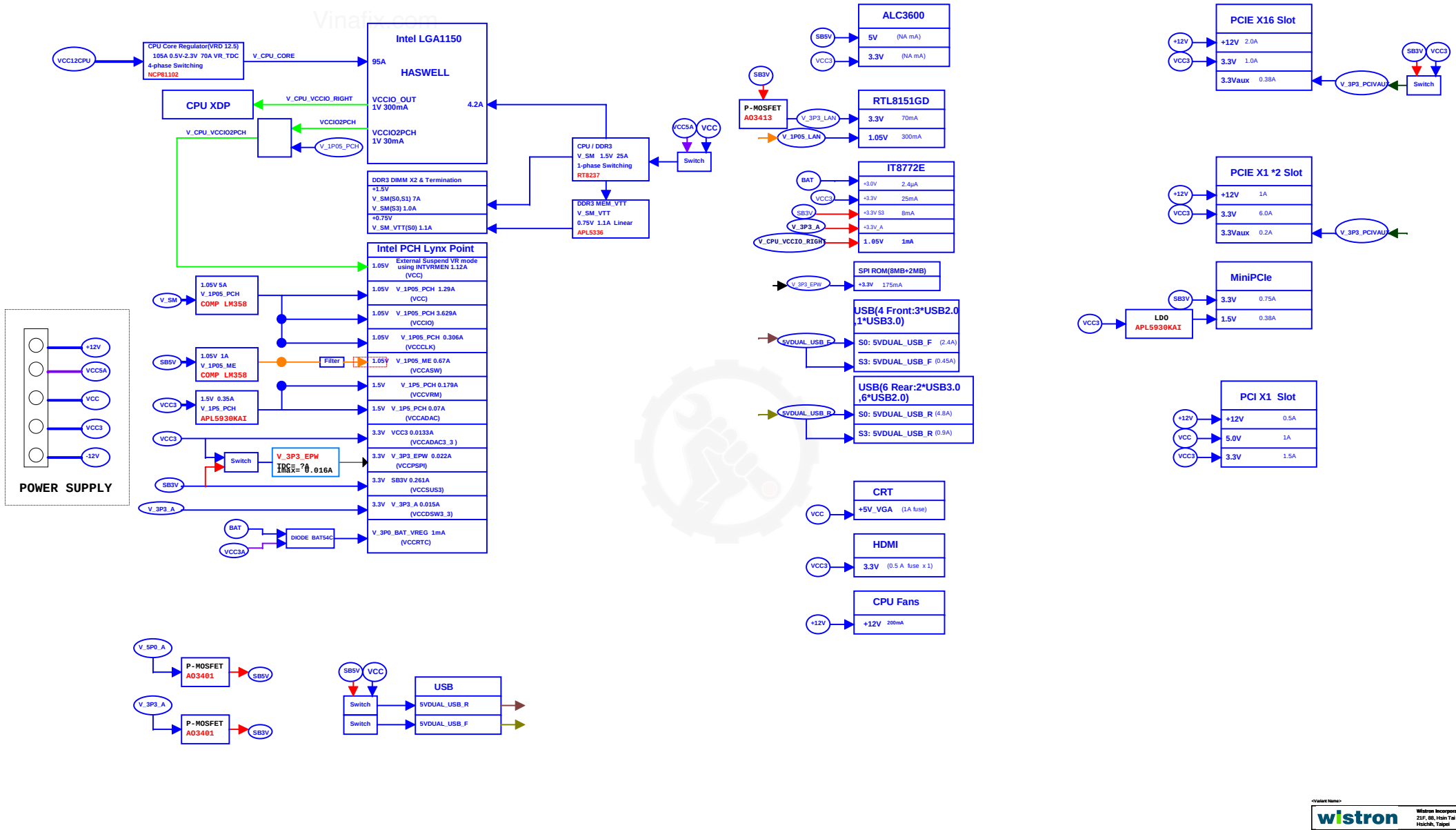
Date: Thursday, August 01, 2013 Sheet 6 of 52



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Document Number
ROSA Shark Bay DTX
Rev SA
Date: Thursday, August 01, 2013
Sheet 7 of 52

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TBD

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TBD

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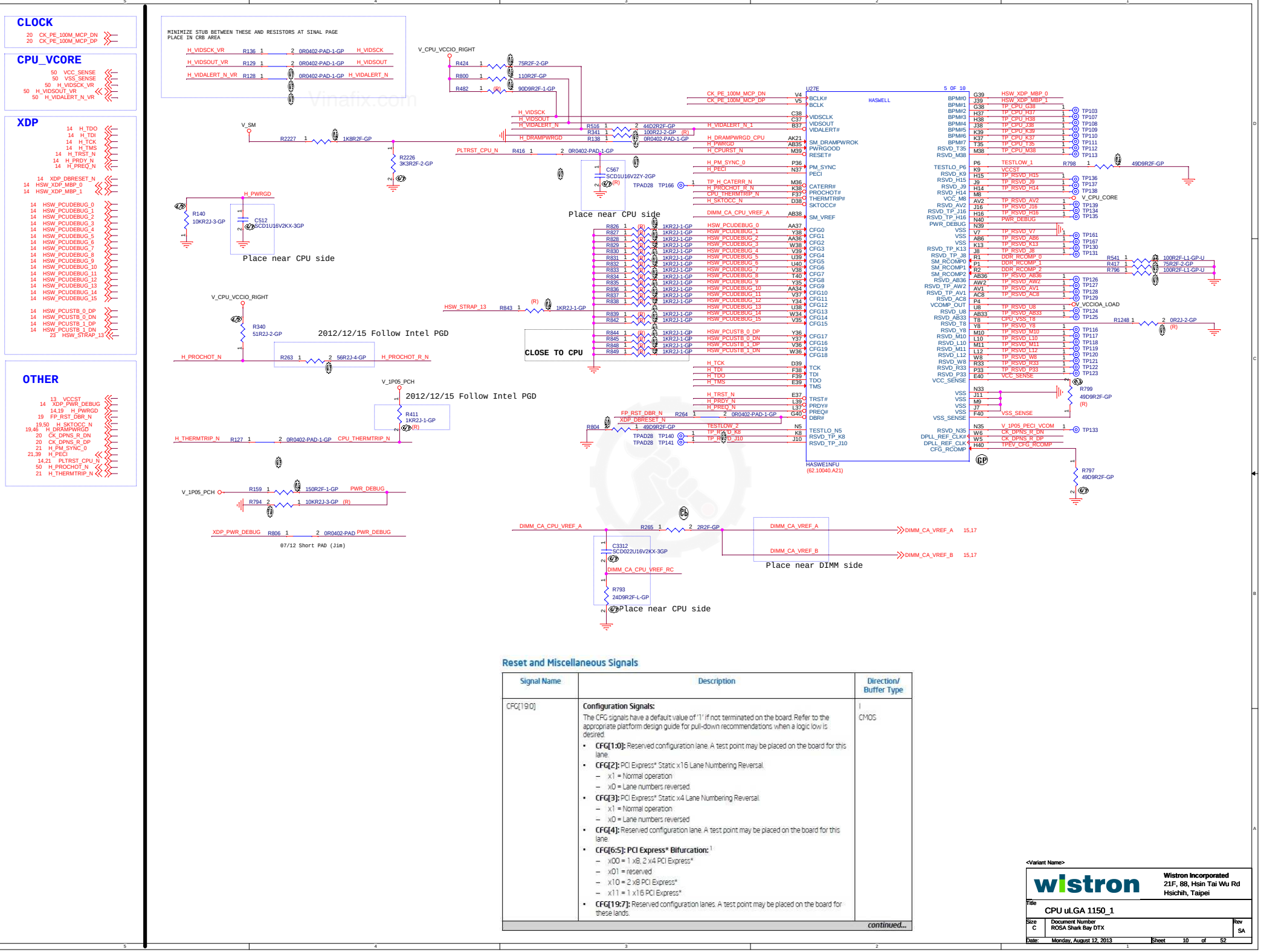
A	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 9 of 52



Reset and Miscellaneous Signals

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[3]:** PCI Express* Static x4 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** [1] – x00 = 1 x8, 2 x4 PCI Express* – x01 = reserved – x10 = 2 x8 PCI Express* – x11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS

continued...

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Title: CPU uLGA 1150_1

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Date: Monday, August 12, 2013 | Sheet 10 of 52

PCIEX16

26 EXP_A_TX_DP[0..15]
26 EXP_A_TX_DN[0..15]

26 EXP_A_RX_DP[0..15]
26 EXP_A_RX_DN[0..15]

DMI

22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]

22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]

FDI

22 FDI_CSYNC
22 FDI_INT
22 FDI_TX_DN[0..1]
22 FDI_TX_DP[0..1]

20 CK_DP_DP
20 CK_DP_DN

HDMI

28 DDSP_C_TX_DP_0
28 DDSP_C_TX_DN_0
28 DDSP_C_TX_DP_1
28 DDSP_C_TX_DN_1
28 DDSP_C_TX_DP_2
28 DDSP_C_TX_DN_2
28 DDSP_C_TX_DP_3
28 DDSP_C_TX_DN_3

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U27C — HASWELL — 3 OF 10

EXP_A_RX_DP0	E15	PEG_RX0	PEG_TX0 A12 EXP_A_TX_DP0
EXP_A_RX_DN0	F15	PEG_RX#0	PEG_TX#0 B12 EXP_A_TX_DN0
EXP_A_RX_DP1	D14	PEG_RX1	PEG_TX1 B11 EXP_A_TX_DP1
EXP_A_RX_DN1	E14	PEG_RX#1	PEG_TX#1 C11 EXP_A_TX_DN1
EXP_A_RX_DP2	E13	PEG_RX2	PEG_TX2 C10 EXP_A_TX_DP2
EXP_A_RX_DN2	F13	PEG_RX#2	PEG_TX#2 D10 EXP_A_TX_DN2
EXP_A_RX_DP3	D12	PEG_RX3	PEG_TX3 B9 EXP_A_TX_DP3
EXP_A_RX_DN3	E12	PEG_RX#3	PEG_TX#3 C9 EXP_A_TX_DN3
EXP_A_RX_DP4	E11	PEG_RX4	PEG_TX4 C8 EXP_A_TX_DP4
EXP_A_RX_DN4	F11	PEG_RX#4	PEG_TX#4 D8 EXP_A_TX_DN4
EXP_A_RX_DP5	F10	PEG_RX5	PEG_TX5 B7 EXP_A_TX_DP5
EXP_A_RX_DN5	G10	PEG_RX#5	PEG_TX#5 C7 EXP_A_TX_DN5
EXP_A_RX_DP6	E9	PEG_RX6	PEG_TX6 A6 EXP_A_TX_DP6
EXP_A_RX_DN6	F9	PEG_RX#6	PEG_TX#6 B6 EXP_A_TX_DN6
EXP_A_RX_DP7	F8	PEG_RX7	PEG_TX7 B5 EXP_A_TX_DP7
EXP_A_RX_DN7	G8	PEG_RX#7	PEG_TX#7 C5 EXP_A_TX_DN7
EXP_A_RX_DP8	D3	PEG_RX8	PEG_TX8 E1 EXP_A_TX_DP8
EXP_A_RX_DN8	D4	PEG_RX#8	PEG_TX#8 E2 EXP_A_TX_DN8
EXP_A_RX_DP9	E4	PEG_RX9	F2 EXP_A_TX_DP9
EXP_A_RX_DN9	E5	PEG_RX#9	F3 EXP_A_TX_DN9
EXP_A_RX_DP10	F5	PEG_RX10	G1 EXP_A_TX_DP10
EXP_A_RX_DN10	F6	PEG_RX#10	G2 EXP_A_TX_DN10
EXP_A_RX_DP11	G4	PEG_RX11	H2 EXP_A_TX_DP11
EXP_A_RX_DN11	G5	PEG_RX#11	H3 EXP_A_TX_DN11
EXP_A_RX_DP12	H5	PEG_RX12	J1 EXP_A_TX_DP12
EXP_A_RX_DN12	H6	PEG_RX#12	J2 EXP_A_TX_DN12
EXP_A_RX_DP13	J4	PEG_RX13	K2 EXP_A_TX_DP13
EXP_A_RX_DN13	J5	PEG_RX#13	K3 EXP_A_TX_DN13
EXP_A_RX_DP14	K5	PEG_RX14	M2 EXP_A_TX_DP14
EXP_A_RX_DN14	K6	PEG_RX#14	M3 EXP_A_TX_DN14
EXP_A_RX_DP15	L4	PEG_RX15	L1 EXP_A_TX_DP15
EXP_A_RX_DN15	L5	PEG_RX#15	L2 EXP_A_TX_DN15
DMI_IT_MR_DP0	U3	DMI_RX0	DMI_TX0 AA4 DMI_MT_IR_DP0
DMI_IT_MR_DN0	T3	DMI_RX#0	DMI_TX#0 AA5 DMI_MT_IR_DN0
DMI_IT_MR_DP1	U1	DMI_RX1	DMI_TX1 AB3 DMI_MT_IR_DP1
DMI_IT_MR_DN1	V1	DMI_RX#1	DMI_TX#1 AB4 DMI_MT_IR_DN1
DMI_IT_MR_DP2	W2	DMI_RX2	DMI_TX2 AC5 DMI_MT_IR_DP2
DMI_IT_MR_DN2	V2	DMI_RX#2	DMI_TX#2 AC4 DMI_MT_IR_DN2
DMI_IT_MR_DP3	Y3	DMI_RX3	DMI_TX3 AC1 DMI_MT_IR_DP3
DMI_IT_MR_DN3	W3	DMI_RX#3	DMI_TX#3 AC2 DMI_MT_IR_DN3

TP35 1 TP_PEG_D1 — D1 RSVD_TP_D1
TP36 1 TP_PEG_C2 — C2 RSVD_TP_C2
TP78 1 TP_PEG_B3 — B3 RSVD_TP_B3
TP79 1 TP_PEG_A4 — A4 RSVD_TP_A4

V_VCCIOA_LOAD — R307 1 — 24D9R2F-L-GP — PEG_COMP — P3 PEG_RCOMP

HASWE1NFU
(62.10040.A21)

U27D — HASWELL — 4 OF 10

FDI_CSYNC	D16	FDI_CSYNC	DDIB_TXB0 E17
FDI_INT	D18	FDI_INT	DDIB_TXB#0 F17
			DDIB_TXB1 F18
			DDIB_TXB#1 G18
			DDIB_TXB2 G19
			DDIB_TXB#2 H19
			DDIB_TXB3 F20
			DDIB_TXB#3 G20
DP_COMP	R4	DP_COMP	
CK_DP_DN	U5	SSC_DPLL_REF_CLK#	
CK_DP_DP	U6	SSC_DPLL_REF_CLK	
DISP_UTIL_CPU	E16	EDP_DISP_UTIL	
TP_DISP_K11	K11	RSVD_TP_K11	
TP_DISP_J12	J12	RSVD_TP_J12	
FDI_TX_DN0	B14	FDI0_TX0#0	DDIC_TXC0 D19 DDSP_C_TX_DP_0
FDI_TX_DP0	A14	FDI0_TX00	DDIC_TXC#0 E19 DDSP_C_TX_DN_0
FDI_TX_DN1	C13	FDI0_TX0#1	DDIC_TXC1 C20 DDSP_C_TX_DP_1
FDI_TX_DP1	B13	FDI0_TX01	DDIC_TXC#1 D20 DDSP_C_TX_DN_1
			DDIC_TXC2 D21 DDSP_C_TX_DP_2
			DDIC_TXC#2 E21 DDSP_C_TX_DN_2
			DDIC_TXC3 C22 DDSP_C_TX_DP_3
			DDIC_TXC#3 D22 DDSP_C_TX_DN_3
			DDID_TXD0 B15
			DDID_TXD#0 C15
			DDID_TXD1 A16
			DDID_TXD#1 B16
			DDID_TXD2 B17
			DDID_TXD#2 C17
			DDID_TXD3 A18
			DDID_TXD#3 B18

HDMI

V_VCCIOA_LOAD — R805 1 — 24D9R2F-L-GP — DP_COMP — R4

TP80 1 DISP_UTIL_CPU — E16
TP77 1 TP_DISP_K11 — K11
TP76 1 TP_DISP_J12 — J12

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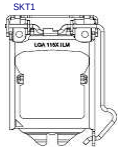
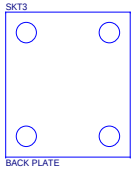
(62.10040.A21)

Add the BACK PLATE
60.3EQ19.001
20120302



Load Plate
(22.78003.021)

Back Plate
(22.78006.031)



BACK PLATE
(60.3EQ19.001)

ILMCOVER
(22.78005.171)

<Variant Name>

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Title: CPU uLGA 1150_2

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Monday, August 19, 2013 Sheet 11 of 52

DDR DATA

15 M_DATA_A[0..63]
17 M_DATA_B[0..63]

15 M_DQS_A_DP[0..7]
15 M_DQS_A_DN[0..7]

17 M_DQS_B_DP[0..7]
17 M_DQS_B_DN[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
17 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

17 M_WE_B_N
17 M_CAS_B_N
17 M_RAS_B_N
17 M_SBS_B0
17 M_SBS_B1
17 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1

15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

17 M_SCS_B_N0
17 M_SCS_B_N1

17 M_SCKE_B0
17 M_SCKE_B1

17 M_ODT_B0
17 M_ODT_B1

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

17 CK_M_DDR0_B_DP
17 CK_M_DDR0_B_DN
17 CK_M_DDR1_B_DN
17 CK_M_DDR1_B_DN

DDR OTHERS

15,17 DDR3_DRAMRST_N

17 DIMM_DQ_CPU_VREF_B
15 DIMM_DQ_CPU_VREF_A

Other

14,19,21,39 PWRGD_3V

U27A — 1 OF 10 — HASWELL

M_DATA_A0	AD38	SA_DQ0	SA_MA0	AU13	M_MAA_A0
M_DATA_A1	AD39	SA_DQ1	SA_MA1	AV16	M_MAA_A1
M_DATA_A2	AF38	SA_DQ2	SA_MA2	AU16	M_MAA_A2
M_DATA_A3	AF39	SA_DQ3	SA_MA3	AW17	M_MAA_A3
M_DATA_A4	AD37	SA_DQ4	SA_MA4	AU17	M_MAA_A4
M_DATA_A5	AD40	SA_DQ5	SA_MA5	AW18	M_MAA_A5
M_DATA_A6	AF37	SA_DQ6	SA_MA6	AV17	M_MAA_A6
M_DATA_A7	AF40	SA_DQ7	SA_MA7	AT18	M_MAA_A7
M_DATA_A8	AH40	SA_DQ8	SA_MA8	AU18	M_MAA_A8
M_DATA_A9	AM39	SA_DQ9	SA_MA9	AT19	M_MAA_A9
M_DATA_A10	AK38	SA_DQ10	SA_MA10	AW11	M_MAA_A10
M_DATA_A11	AK39	SA_DQ11	SA_MA11	AV19	M_MAA_A11
M_DATA_A12	AH37	SA_DQ12	SA_MA12	AU19	M_MAA_A12
M_DATA_A13	AH38	SA_DQ13	SA_MA13	AY10	M_MAA_A13
M_DATA_A14	AK37	SA_DQ14	SA_MA14	AT20	M_MAA_A14
M_DATA_A15	AK40	SA_DQ15	SA_MA15	AU21	M_MAA_A15
M_DATA_A16	AM40	SA_DQ16			
M_DATA_A17	AM38	SA_DQ17	SA_ODT0	AW10	M_ODT_A0
M_DATA_A18	AP38	SA_DQ18	SA_ODT1	AY8	M_ODT_A1
M_DATA_A19	AP39	SA_DQ19	SA_ODT2	AW9	
M_DATA_A20	AM37	SA_DQ20	SA_ODT3	AU8	
M_DATA_A21	AM38	SA_DQ21			
M_DATA_A22	AP37	SA_DQ22			
M_DATA_A23	AP40	SA_DQ23	SA_ECC_CB0	AW33	
M_DATA_A25	AV37	SA_DQ24	SA_ECC_CB1	AV33	
M_DATA_A29	AW37	SA_DQ25	SA_ECC_CB2	AU33	
M_DATA_A26	AU35	SA_DQ26	SA_ECC_CB3	AV31	
M_DATA_A27	AV35	SA_DQ27	SA_ECC_CB4	AT33	
M_DATA_A28	AT37	SA_DQ28	SA_ECC_CB5	AU31	
M_DATA_A24	AU37	SA_DQ29	SA_ECC_CB6	AT31	
M_DATA_A30	AT35	SA_DQ30	SA_ECC_CB7	AW31	
M_DATA_A31	AW35	SA_DQ31			
M_DATA_A33	AY6	SA_DQ32	SA_BS0	AV12	M_SBS_A0
M_DATA_A37	AU6	SA_DQ33	SA_BS1	AY11	M_SBS_A1
M_DATA_A34	AV4	SA_DQ34	SA_BS2	AT21	M_SBS_A2
M_DATA_A35	AU4	SA_DQ35			
M_DATA_A36	AW6	SA_DQ36	SA_CKE0	AV22	M_SCKE_A0
M_DATA_A32	AV6	SA_DQ37	SA_CKE1	AT23	M_SCKE_A1
M_DATA_A38	AW4	SA_DQ38	SA_CKE2	AU22	
M_DATA_A39	AY4	SA_DQ39	SA_CKE3	AU23	
M_DATA_A41	AR1	SA_DQ40			
M_DATA_A45	AR4	SA_DQ41	SA_CS#0	AU14	M_SCS_A_N0
M_DATA_A42	AN3	SA_DQ42	SA_CS#1	AV9	M_SCS_A_N1
M_DATA_A43	AN4	SA_DQ43	SA_CS#2	AU10	
M_DATA_A44	AP2	SA_DQ44	SA_CS#3	AW8	
M_DATA_A40	AR3	SA_DQ45			
M_DATA_A46	AN2	SA_DQ46	SA_CK0	AY15	CK_M_DDR0_A_DP
M_DATA_A47	AN1	SA_DQ47	SA_CK#0	AY16	CK_M_DDR0_A_DN
M_DATA_A49	AL1	SA_DQ48	SA_CK1	AW15	CK_M_DDR1_A_DP
M_DATA_A53	AL4	SA_DQ49	SA_CK#1	AV15	CK_M_DDR1_A_DN
M_DATA_A50	AJ3	SA_DQ50	SA_CK2	AV14	
M_DATA_A51	AJ4	SA_DQ51	SA_CK#2	AW16	
M_DATA_A52	AL2	SA_DQ52	SA_CK3	AW13	
M_DATA_A48	AL3	SA_DQ53	SA_CK#3	AY13	
M_DATA_A54	AJ2	SA_DQ54			
M_DATA_A55	AJ1	SA_DQ55	RSVD_AW12	AW12	TP_RSVD_AW12 1 — TP34
M_DATA_A57	AG1	SA_DQ56			
M_DATA_A61	AG4	SA_DQ57			
M_DATA_A58	AE3	SA_DQ58			
M_DATA_A59	AE4	SA_DQ59			
M_DATA_A60	AG2	SA_DQ60			
M_DATA_A56	AG3	SA_DQ61			
M_DATA_A62	AE2	SA_DQ62			
M_DATA_A63	AE1	SA_DQ63			
M_DQS_A_DP0	AE39	SA_DQS0			
M_DQS_A_DP1	AJ39	SA_DQS1			
M_DQS_A_DP2	AN39	SA_DQS2			
M_DQS_A_DP3	AV39	SA_DQS3			
M_DQS_A_DP4	AV5	SA_DQS4			
M_DQS_A_DP5	AP3	SA_DQS5			
M_DQS_A_DP6	AK3	SA_DQS6			
M_DQS_A_DP7	AF3	SA_DQS7			
	AV32	SA_DQS8			
M_DQS_A_DN0	AE38	SA_DQS#0			
M_DQS_A_DN1	AJ38	SA_DQS#1			
M_DQS_A_DN2	AN38	SA_DQS#2			
M_DQS_A_DN3	AU36	SA_DQS#3			
M_DQS_A_DN4	AW5	SA_DQS#4			
M_DQS_A_DN5	AP2	SA_DQS#5			
M_DQS_A_DN6	AK2	SA_DQS#6			
M_DQS_A_DN7	AF2	SA_DQS#7			
	AU32	SA_DQS#8			
			SA_RAS#	AU12	M_RAS_A_N
			SA_WE#	AU11	M_WE_A_N
			RSVD_AV20	AV20	TP_RSVD_AV20 1 — TP32
			RSVD_AW27	AW27	TP_RSVD_AW27 1 — TP33
			SA_CAS#	AU9	M_CAS_A_N
			SM_DRAMRST#	AK22	DDR3_DRAMRST_N

HASWE1NFU (62.10040.A21)

CS20 SCD1U16V2KX-3GP

U27B — 2 OF 10 — HASWELL

M_DATA_B0	AE34	SB_DQ0	SB_MA0	AL19	M_MAA_B0
M_DATA_B1	AE35	SB_DQ1	SB_MA1	AK23	M_MAA_B1
M_DATA_B2	AG35	SB_DQ2	SB_MA2	AM22	M_MAA_B2
M_DATA_B3	AH35	SB_DQ3	SB_MA3	AM23	M_MAA_B3
M_DATA_B4	AD34	SB_DQ4	SB_MA4	AP23	M_MAA_B4
M_DATA_B5	AD35	SB_DQ5	SB_MA5	AL23	M_MAA_B5
M_DATA_B6	AG34	SB_DQ6	SB_MA6	AY24	M_MAA_B6
M_DATA_B7	AH34	SB_DQ7	SB_MA7	AV25	M_MAA_B7
M_DATA_B8	AL34	SB_DQ8	SB_MA8	AU26	M_MAA_B8
M_DATA_B9	AL35	SB_DQ9	SB_MA9	AW25	M_MAA_B9
M_DATA_B10	AK31	SB_DQ10	SB_MA10	AP18	M_MAA_B10
M_DATA_B11	AL31	SB_DQ11	SB_MA11	AY25	M_MAA_B11
M_DATA_B12	AK34	SB_DQ12	SB_MA12	AV26	M_MAA_B12
M_DATA_B13	AK35	SB_DQ13	SB_MA13	AR15	M_MAA_B13
M_DATA_B14	AK32	SB_DQ14	SB_MA14	AV27	M_MAA_B14
M_DATA_B15	AL32	SB_DQ15	SB_MA15	AY28	M_MAA_B15
M_DATA_B17	AN34	SB_DQ16			
M_DATA_B21	AP34	SB_DQ17	SB_ODT0	AM17	M_ODT_B0
M_DATA_B19	AN31	SB_DQ18	SB_ODT1	AL16	M_ODT_B1
M_DATA_B23	AP31	SB_DQ19	SB_ODT2	AM16	
M_DATA_B20	AN35	SB_DQ20	SB_ODT3	AK15	
M_DATA_B16	AP35	SB_DQ21			
M_DATA_B18	AN32	SB_DQ22	SB_ECC_CB0	AM26	
M_DATA_B22	AP32	SB_DQ23	SB_ECC_CB1	AM25	
M_DATA_B25	AM29	SB_DQ24	SB_ECC_CB2	AP25	
M_DATA_B28	AM28	SB_DQ25	SB_ECC_CB3	AP26	
M_DATA_B27	AR29	SB_DQ26	SB_ECC_CB4	AL26	
M_DATA_B30	AR28	SB_DQ27	SB_ECC_CB5	AL25	
M_DATA_B24	AL29	SB_DQ28	SB_ECC_CB6	AR25	
M_DATA_B29	AL28	SB_DQ29	SB_ECC_CB7	AR26	
M_DATA_B26	AP29	SB_DQ30			
M_DATA_B31	AP28	SB_DQ31			
M_DATA_B32	AR12	SB_DQ32	SB_BS0	AK17	M_SBS_B0
M_DATA_B33	AP12	SB_DQ33	SB_BS1	AL18	M_SBS_B1
M_DATA_B34	AL13	SB_DQ34	SB_BS2	AW28	M_SBS_B2
M_DATA_B35	AL12	SB_DQ35			
M_DATA_B36	AR13	SB_DQ36	SB_CKE0	AW29	M_SCKE_B0
M_DATA_B37	AP13	SB_DQ37	SB_CKE1	AY29	M_SCKE_B1
M_DATA_B38	AM13	SB_DQ38	SB_CKE2	AU28	
M_DATA_B39	AM12	SB_DQ39	SB_CKE3	AU29	
M_DATA_B45	AR9	SB_DQ40			
M_DATA_B41	AP9	SB_DQ41			
M_DATA_B47	AR6	SB_DQ42			
M_DATA_B43	AP6	SB_DQ43			
M_DATA_B44	AR10	SB_DQ44	SB_CS#0	AP17	M_SCS_B_N0
M_DATA_B40	AP10	SB_DQ45	SB_CS#1	AN15	M_SCS_B_N1
M_DATA_B46	AR7	SB_DQ46	SB_CS#2	AN17	
M_DATA_B42	AP7	SB_DQ47	SB_CS#3	AL15	
M_DATA_B52	AM9	SB_DQ48			
M_DATA_B53	AL9	SB_DQ49	SB_CK0	AM20	CK_M_DDR0_B_DP
M_DATA_B50	AL6	SB_DQ50	SB_CK#0	AM21	CK_M_DDR0_B_DN
M_DATA_B55	AL7	SB_DQ51	SB_CK1	AP22	CK_M_DDR1_B_DP
M_DATA_B48	AM10	SB_DQ52	SB_CK#1	AP21	CK_M_DDR1_B_DN
M_DATA_B49	AL10	SB_DQ53			
M_DATA_B54	AM6	SB_DQ54	SB_CK2	AN20	
M_DATA_B51	AM7	SB_DQ55	SB_CK#2	AN21	
M_DATA_B61	AH6	SB_DQ56	SB_CK3	AH19	
M_DATA_B60	AH7	SB_DQ57	SB_CK#3	AP20	
M_DATA_B59	AE6	SB_DQ58			
M_DATA_B63	AE7	SB_DQ59	SB_CAS#	AP16	M_CAS_B_N
M_DATA_B56	AJ6	SB_DQ60	RSVD_AL20	AL20	
M_DATA_B57	AJ7	SB_DQ61	SB_RAS#	AM18	M_RAS_B_N
M_DATA_B58	AF6	SB_DQ62	SB_WE#	AK16	M_WE_B_N
M_DATA_B62	AF7	SB_DQ63			
M_DQS_B_DP0	AF35	SB_DQS0	SA_DIMM_VREFDQ	AB39	DIMM_DQ_CPU_VREF_A
M_DQS_B_DP1	AL33	SB_DQS1	SB_DIMM_VREFDQ	AB40	DIMM_DQ_CPU_VREF_B
M_DQS_B_DP2	AP33	SB_DQS2			
M_DQS_B_DP3	AP28	SB_DQS3			
M_DQS_B_DP4	AN12	SB_DQS4			
M_DQS_B_DP5	AP8	SB_DQS5			
M_DQS_B_DP6	AL8	SB_DQS6			
M_DQS_B_DP7	AG7	SB_DQS7			
	AN25	SB_DQS8			
M_DQS_B_DN0	AF34	SB_DQS#0			
M_DQS_B_DN1	AK33	SB_DQS#1			
M_DQS_B_DN2	AN33	SB_DQS#2			
M_DQS_B_DN3	AN29	SB_DQS#3			
M_DQS_B_DN4	AN13	SB_DQS#4			
M_DQS_B_DN5	AR8	SB_DQS#5			
M_DQS_B_DN6	AM8	SB_DQS#6			
M_DQS_B_DN7	AG6	SB_DQS#7			
	AN26	SB_DQS#8			

HASWE1NFU (62.10040.A21)

U27H — 8 OF 10 — HASWELL

PWRGD_3V

R2230 (R) 6K04R2F-GP

R2231 (R) 2K67R2F-2-GP

TP148	TP_RSVD_AY18	AY18	RSVD_AY18
TP149	TP_RSVD_AW24	AW24	RSVD_AW24
TP150	TP_RSVD_AW23	AW23	RSVD_AW23
TP151	TP_RSVD_AV29	AV29	RSVD_AV29
TP152	TP_RSVD_AV24	AV24	RSVD_AV24
TP153	TP_RSVD_AU39	AU39	RSVD_AU39
TP154	TP_RSVD_AU27	AU27	RSVD_AU27
TP155	TP_RSVD_AU1	AU1	RSVD_AU1
TP164	TP_RSVD_AT40	AT40	RSVD_AT40
TP160	TP_RSVD_AK20	AK20	RSVD_AK20
	VCCST_PWRGD	Y7	RSVD_Y7
TP162	TP_RSVD_T34	T34	RSVD_T34
TP163	TP_RSVD_R34	R34	RSVD_R34
TP156	TP_RSVD_J40	J40	RSVD_J40
TP157	TP_RSVD_J17	J17	RSVD_J17
TP158	TP_RSVD_J15	J15	RSVD_J15
TP159	TP_RSVD_H12	H12	RSVD_H12

K12	TP_RSVD_K12	TP142	RSVD_TP_K12
J13	TP_RSVD_J13	TP143	RSVD_TP_J13
P37	TP_RSVD_P37	TP144	RSVD_TP_P37
N38	TP_RSVD_N38	TP145	RSVD_TP_N38
R36	TP_RSVD_R36	TP146	RSVD_TP_R36
C39	TP_RSVD_C39	TP147	RSVD_TP_C39
U35			VSS
P40			VSS
R38			VSS
T37			VSS
V34			VSS
R39			VSS
T38			VSS
U36			VSS
P39			VSS
T36			VSS
R37			VSS
J14			VSS
N36	TP_CPU_N36	TP165	RSVD_TP_N36

HASWE1NFU (62.10040.A21)

<Variant Name>

wistron

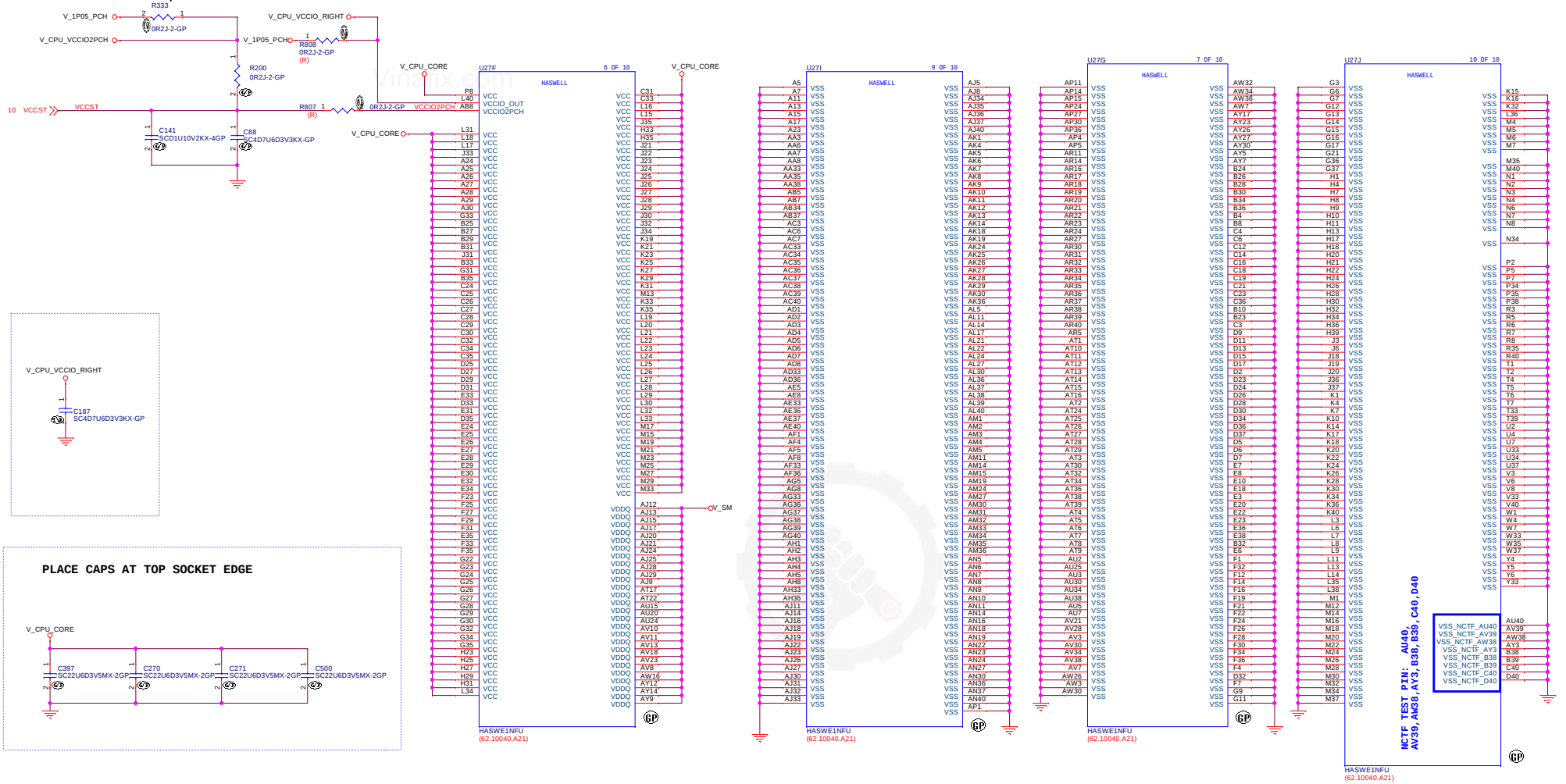
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU uLGA 1150_3

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Monday, August 12, 2013 Sheet 12 of 52

Put R333 near PCH side for V_CPU_VCCIO2PCH is for PCH power



DEFENSIVE DESIGN PWR_DEBUG

2012/12/04 Ryan removed,

CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	22
V_SM	22uf 0805	4+5(R)

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU uLGA 1150_4

Size: Custom | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Monday, August 19, 2013 | Sheet 13 of 52

XDP for CPU

10 H_TDO
10 H_TDI
10 H_TMS
10 H_TCK
10 H_TRST_N
10 H_PREQ_N
10 H_PRDY_N
10 XDP_DBRESET_N
10,19 H_PWRGD

10 HSW_PCUDEBUG_0
10 HSW_PCUDEBUG_1
10 HSW_PCUDEBUG_2
10 HSW_PCUDEBUG_3
10 HSW_PCUDEBUG_4
10 HSW_PCUDEBUG_5
10 HSW_PCUDEBUG_6
10 HSW_PCUDEBUG_7
10 HSW_PCUDEBUG_8
10 HSW_PCUDEBUG_9
10 HSW_PCUDEBUG_10
10 HSW_PCUDEBUG_11
10 HSW_PCUDEBUG_12
10 HSW_PCUDEBUG_13
10 HSW_PCUDEBUG_14
10 HSW_PCUDEBUG_15

10 HSW_XDP_MBP_0
10 HSW_XDP_MBP_1

10 HSW_PCUSTB_0_DP
10 HSW_PCUSTB_0_DN
10 HSW_PCUSTB_1_DP
10 HSW_PCUSTB_1_DN

10 XDP_PWR_DEBUG

15,17,39 SMB_DATA_MAIN
15,17,39 SMB_CLK_MAIN

20 CK_100M_CPU_XDP_DN
20 CK_100M_CPU_XDP_DP

19,39 SW_ON_N

10,21 PLTRST_CPU_N

XDP for PCH

19 PCH_JTAG_RST_R
19 PCH_JTAG_TDO
19 PCH_JTAG_TDI
19 PCH_JTAG_TMS
19 PCH_JTAG_TCK

19,50 VR_READY
12,19,21,39 PWRGD_3V

LPC DEBUG PORT

19,39 L_AD0
19,39 L_AD1
19,39 L_AD2
19,39 L_AD3
19,39 L_FRAME_N
20 CK_P_33M_LPCP80
39 PCIRST3#

XDP for CPU

PLace Near XDP_CONN
V_CPU_VCCIO_RIGHT
R640 1 (R) 51R2J-2-GP H_TDI
PLace Near CPU
R639 1 (R) 51R2J-2-GP H_TMS
R663 1 (R) 51R2J-2-GP H_TCK
H_TCK TERMINATION PLACE NEAR CPU WITHIN 1.1 INCH
R661 1 2 51R2J-2-GP H_TRST_N
PLace Any where

PLTRST_CPU_N R660 1 (P) 1KR2J-1-GP H_RSTOUT_XDP_N
VR_READY R819 1 (P) 0R2J-2-GP XDP_VR_READY

H_PWRGD R519 1 (P) 1KR2J-1-GP XDP_PWRGD
R518 1KR2F-3-GP (R)

SW_ON_N R637 1 (P) 0R2J-2-GP XDP_PLTRST_N

V_1P05_PCH
VCC3
R2216 51R2F-2-GP
(R) R2218 249R2F-GP H_TDO
(R) R2217 825R2F-GP
(R) R2219 100R2F-L1-GP-U
PLace Near XDP CONN

V_CPU_VCCIO_RIGHT
XDPC1
MH1
V_CPU_VCCIO_RIGHT
H_PREQ_N
H_PRDY_N
HSW_PCUDEBUG_0
HSW_PCUDEBUG_1
HSW_PCUDEBUG_2
HSW_PCUDEBUG_3
HSW_XDP_MBP_0
HSW_XDP_MBP_1
HSW_PCUDEBUG_4
HSW_PCUDEBUG_5
HSW_PCUDEBUG_6
HSW_PCUDEBUG_7
XDP_PWRGD
XDP_PLTRST_N
XDP_PWR_DEBUG
XDP_VR_READY
SMB_DATA_MAIN
SMB_CLK_MAIN
H_TCK
HSW_PCUSTB_0_DP
HSW_PCUSTB_0_DN
HSW_PCUDEBUG_8
HSW_PCUDEBUG_9
HSW_PCUDEBUG_10
HSW_PCUDEBUG_11
HSW_PCUSTB_1_DP
HSW_PCUSTB_1_DN
HSW_PCUDEBUG_12
HSW_PCUDEBUG_13
HSW_PCUDEBUG_14
HSW_PCUDEBUG_15
CK_XDP_S_DP
CK_XDP_S_DN
H_RSTOUT_XDP_N
XDP_DBRESET_N
H_TDO
H_TRST_N
H_TDI
H_TMS
PRIVACY_MSR_EN_N
MH2
(P)
SMC-CONN60A-GP
R867 1 (P) 1KR2J-1-GP HSW_PCUDEBUG_3

CK_100M_CPU_XDP_DN R820 1 (P) 0R2J-2-GP CK_XDP_S_DN
CK_100M_CPU_XDP_DP R821 1 (P) 0R2J-2-GP CK_XDP_S_DP

XDP_DBRESET_N
C576 SCD1U10V2KX-4GP (P)

LPC DEBUG PORT

VCC3
R638 4K7R2J-2-GP
LPC1
CK_P_33M_LPCP80 INIT_3V
PCIRST3#
L_AD0 FWH_ID0
L_AD1 VCC3
L_AD2 VCC
L_AD3
L_FRAME_N
JWT-CONN14A-S3-GP (P)
R662 10KR2J-3-GP (R)
Pin height 2.3mm

XDP for PCH

Stuff 200 ohm for ES2
Empty for production

SB3V
R811 1 200R2F-L-GP PCH_JTAG_TDO
R817 1 200R2F-L-GP PCH_JTAG_TDI
R766 1 200R2F-L-GP PCH_JTAG_TMS

C575 2 1 SCD1U16V2ZY-2GP (R)
R816 2 1 51R2J-2-GP PCH_JTAG_TCK

R818 100R2F-L1-GP-U
R764 100R2F-L1-GP-U
R812 100R2F-L1-GP-U

PCH_JTAG_TDO 1 TP87 TPAD28
PCH_JTAG_TDI 1 TP105 TPAD28
PCH_JTAG_TMS 1 TP104 TPAD28

SB3V
R765 20KR2J-L2-GP
PCH_JTAG_RST_R
C1672 SC1U10V2KX-1GP (R)
R712 10KR2J-3-GP (R)

SB3V
PWRGD_3V R810 1 (R) 1KR2J-1-GP

2012/12/15 delete reserve R815

All parts can be placed at back side

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: XDP/80 PORT HEADER/APS

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 14 of 52

DDR DATA

12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

DDR OTHERS

14,17,39 SMB_DATA_MAIN
14,17,39 SMB_CLK_MAIN
12,17 DDR3_DRAMRST_N
12 DIMM_DQ_CPU_VREF_A
10,17 DIMM_CA_VREF_A

DIMM1A 1 OF 3

DDR3-240P-4-GP
(022.10010.0001)
Black color
Pin Height is 2.7mm

Trace: 12/12 mils

DIMM1C 3 OF 3

DM8 must connect to GND

DDR3-240P-4-GP
(022.10010.0001)

DIMM1B 2 OF 3

DDR3-240P-4-GP
(022.10010.0001)

CHANNEL A DIMM1

SMB ADDRESS: 000
SPD R/W: 0*A1, 0*A0

DIMM VREF DQ A (To DIMM/CPU)

DIMM VREF CA A (To DIMM)

05/02 Overshoot solution

Place Near DIMM CONN

Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 X5R	5+4
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 X5R	1

CAPS FOR DIMM

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR3 CHA DIMM 0

Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Wednesday, August 28, 2013 | Sheet 15 of 52

Vinafix.com

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

TBD

Size	Document Number	Rev
A	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 16 of 52

DDR DATA

12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2

DDR CTRL

12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN

DDR OTHERS

14,15,39 SMB_DATA_MAIN
14,15,39 SMB_CLK_MAIN
12,15 DDR3_DRAMRST_N
12 DIMM_DQ_CPU_VREF_B
10,15 DIMM_CA_VREF_B

DIMM2A 1 OF 3

DDR3-240P-4-GP
(022.10010.0001)
Black color
Pin Height is 2.7mm

Trace: 12/12 mils

DIMM2C 3 OF 3

DM8 must connect to GND

DDR3-240P-4-GP
(022.10010.0001)

DIMM2B 2 OF 3

DDR3-240P-4-GP
(022.10010.0001)

CHANNEL B DIMM1

SMB ADDRESS: 010

SPD R/W: 0*A5, 0*A4

DIMM VREF DQ B (To DIMM/CPU)

DIMM VREF CA B (To DIMM)

Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 X5R	9
V_SM	1uf 0402 X5R	5
V_SM_VTT	0.1uf 0402 X5R	1
V_SM_VTT	4.7uf 0603 X5R	1

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR3 CHB DIMM 0

Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Wednesday, August 07, 2013 | Sheet 17 of 52

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<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

TBD

Size	Document Number	Rev
A	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 18 of 52

LPC

14,39 L_AD0
14,39 L_AD1
14,39 L_AD2
14,39 L_AD3
14,39 L_FRAME_N

HD LINK

36 AUD_LINK_BCLK
36 AUD_LINK_RST_N
36 AUD_LINK_SDIN
36 AUD_LINK_SDO
36 AUD_LINK_SYNC
23 AUD_LINK_SDO_R

SMBUS

26,39,42,43,44 SMB_CLK_RESUME
26,39,42,43,44 SMB_DATA_RESUME
39 SMLICLK_PCH
39 SMLIDATA_PCH

JTAG

14 PCH_JTAG_RST_R
14 PCH_JTAG_TCK
14 PCH_JTAG_TDI
14 PCH_JTAG_TDO
14 PCH_JTAG_TMS

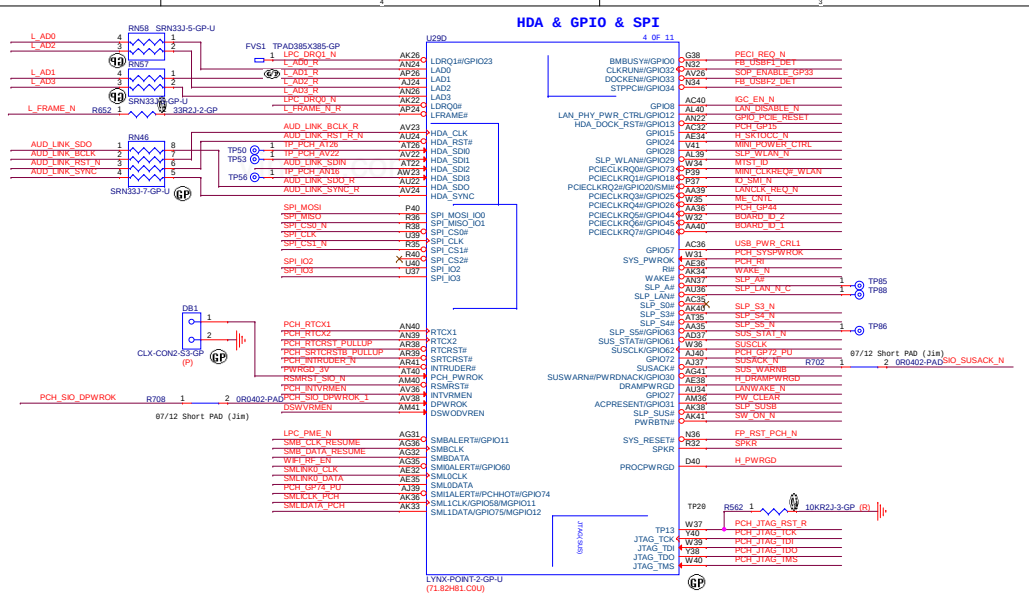
PWR MANAGER

10,46 H_DRAMPWRGD
10,14 H_PWRGD
10 FP_RST_DBR_N
12,14,21,39 PWRGD_3V
39 RSMRST_SIO_N
14,50 VR_READY
39,46,48,50 SLP_S3_N
39,45,47 SLP_S4_N
14,39 SW_ON_N

GPIO/MISC

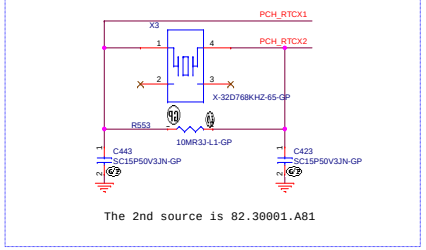
10,50 H_SKTOCC_N
23 PCH_INTVRMEN
39 PCH_SIO_DPWROK
23 DSWVRMEN
39 LPC_PME_N
43 WIFI_RF_EN
34 FB_USBF1_DET
23 IGC_EN_N
35 LAN_DISABLE_N
26 GPIO_PCIE_RESET
23 PCH_GP15
46 MINI_POWER_CTRL
45 MTST_ID
43 MINI_CLKREQ#_WLAN
39 IO_SMI_N
35 LANCLK_REQ_N
22 BOARD_ID_1
22 BOARD_ID_2
46 USB_PWR_CRL1
26,35,38,42,43 WAKE_N
23 SUSCLK
39 SIO_SUSACK_N
39,46 SUS_WARNB
48 SLP_SUSB
23,36 SPKR
30 FB_USBF2_DET

HDA & GPIO & SPI



2012/12/17 change R395 from 100ohm to 10K.

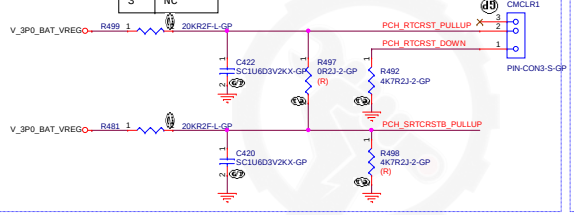
2012/12/17 change R554 from 10K to 100 ohm.



The 2nd source is 82.30001.A81

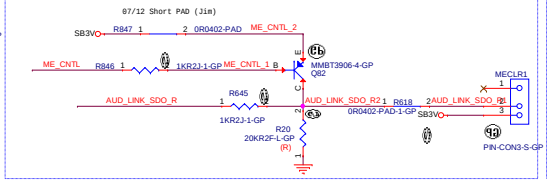
CLEAN CMOS

1	GND
2	RTC_RST
3	NC



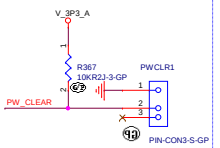
ME ENABLE/DISABLE

1	NC
2	AUD_LINK_SDO_R1
3	SB3V



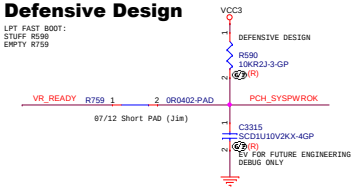
PASSWORD CLEAR

1-2	CLR PASSWORD
2-3	NORMAL(DEFAULT)



Defensive Design

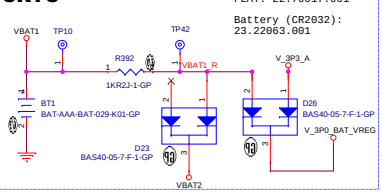
LPT FAST BOOT:
STUFF R590
EMPTY R759



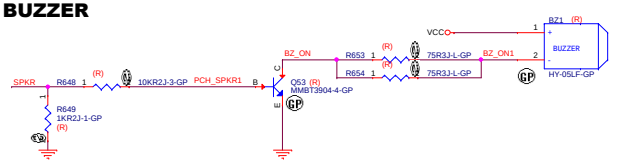
VCCRTC

Battery Socket
ST: 22.70017.051
FLAT: 22.70017.061

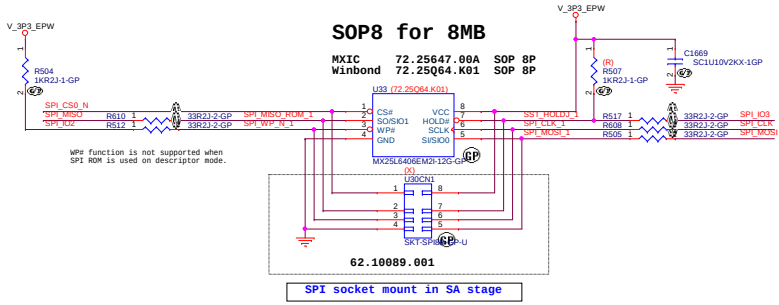
Battery (CR2032):
23.22063.001

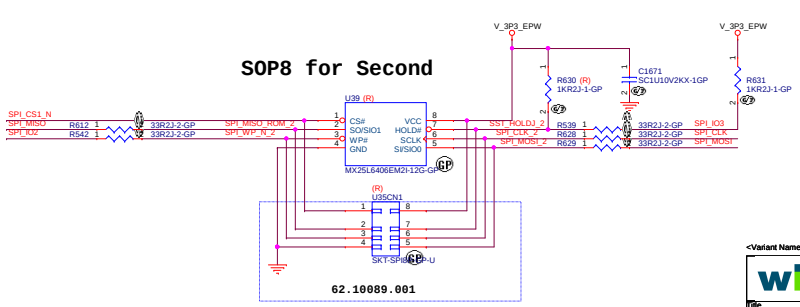


BUZZER



SPI ROM





<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_AUDIO/GPIO/SPI

Size: Custom | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Tuesday, August 06, 2013 | Sheet 19 of 52

CPU CLOCK

10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP

PCI CLOCK

14 CK_P_33M_LPCP80
22 CK_PCH_33M_FB
39 CK_P_33M_SIO

PCIE CLOCK

10 CK_DPNS_R_DN
10 CK_DPNS_R_DP

11 CK_DP_DN
11 CK_DP_DP

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

26 CK_PE_100M_16PORT_DN
26 CK_PE_100M_16PORT_DP

35 CK_GLAN_DN
35 CK_GLAN_DP

43 CK_PCIEX1_WLAN_DN
43 CK_PCIEX1_WLAN_DP

42 CK_PCIE_1PCIEX1_DN
42 CK_PCIE_1PCIEX1_DP

38 CK_PCIE_PCI6_DN
38 CK_PCIE_PCI6_DP

42 CK_PCIE_2PCIEX1_DN
42 CK_PCIE_2PCIEX1_DP

14M CLOCK

39 CK_48M_SIO2

GPIO

43 BT_RADIO_CL

CK_33M_PCI0
CK_33M_PCI1
CK_33M_PCI2
CK_33M_PCI3
CK_48M_PCH
CK_14M_FLEX3

C3316 SC22P50V2JN-4GP (R)
C3322 SC22P50V2JN-4GP (R)
C3317 SC22P50V2JN-4GP (R)
C3318 SC22P50V2JN-4GP (R)
C3319 SC22P50V2JN-4GP (R)
C3323 SC22P50V2JN-4GP (R)

U29G
7 OF 11

CK_P_33M_LPCP80 R408 22R2J-2-GP CK_33M_PCI0 AV5 CLKOUT_33MHZ0
CK_33M_PCI1 AV7 CLKOUT_33MHZ1
CK_PCH_33M_FB R396 22R2J-2-GP CK_33M_PCI2 AU2 CLKOUT_33MHZ2
CK_P_33M_SIO R406 22R2J-2-GP CK_33M_PCI3 AN9 CLKOUT_33MHZ3
AU5 CLKOUT_33MHZ4

CK_48M_SIO2 R407 22R2J-2-GP CK_48M_PCH AV8 CLKOUTFLEX0/GPIO64
BT_RADIO_CL AT9 CLKOUTFLEX1/GPIO65
CK_14M_FLEX3 AV9 CLKOUTFLEX2/GPIO66
AU8 CLKOUTFLEX3/GPIO67

V_1P5_PCH R547 7K5R2F-1DL-GP XCLK_RCOMP R11 DIFFCLK_BIASREF
R410 10KR2J-3-GP CK_REFCLK_PCH AR7 REFCLK14IN

XTAL_25M_PCH_IN R430 1MR3F-GP XTAL_25M_PCH_OUT
N7 XTAL25_IN
N6 XTAL25_OUT
X2 XTAL-25MHZ-102-GP
C379 SC12P50V2JN-3GP
C378 SC12P50V2JN-3GP

LYNX-POINT-2-GP-U
(71.82H81.C0U)

CLKIN_GND0#/CLKIN_GND0_P: G16 / F16 — CK_CSI_PCH_IN_DN / CK_CSI_PCH_IN_DP — RN31 SRN10KJ-5-GP
CLKOUT_DMI#/CLKOUT_DMI_P: R2 / T2 — CK_PE_100M_MCP_DN / CK_PE_100M_MCP_DP — **CLK OUT TO CPU for DMI**
CLKOUT_DP#/CLKOUT_DP_P: T3 / T5 — CK_DP_DN / CK_DP_DP — **CLK OUT TO CPU**
CLKOUT_DPNS#/CLKOUT_DPNS_P: W2 / U2 — CK_DPNS_R_DN / CK_DPNS_R_DP — **CLK OUT TO CPU**
CLKOUT_ITPXDP#/CLKOUT_ITPXDP_P: U6 / U7 — CK_100M_CPU_XDP_DN / CK_100M_CPU_XDP_DP — **CLK OUT TO XDP**
CLKOUT_PEG_A#/CLKOUT_PEG_A_P: AA3 / AA2 — CK_PE_100M_16PORT_DN / CK_PE_100M_16PORT_DP — **CLK OUT TO X16 Graphic**
CLKOUT_PEG_B#/CLKOUT_PEG_B_P: AE6 / AE7
CLKOUT_PCIE_N0/CLKOUT_PCIE_P0: AE10 / AE11
CLKOUT_PCIE_N1/CLKOUT_PCIE_P1: AC6 / AC7
CLKOUT_PCIE_N2/CLKOUT_PCIE_P2: AC11 / AC10 — CK_GLAN_DN / CK_GLAN_DP — **CLK OUT TO PCIEX1 for LAN**
CLKOUT_PCIE_N3/CLKOUT_PCIE_P3: W11 / W10
CLKOUT_PCIE_N4/CLKOUT_PCIE_P4: Y4 / Y2 — CK_PCIE_2PCIEX1_DN / CK_PCIE_2PCIEX1_DP — **CLK OUT TO PCIEX1**
CLKOUT_PCIE_N5/CLKOUT_PCIE_P5: W7 / W6 — CK_PCIEX1_WLAN_DN / CK_PCIEX1_WLAN_DP — **CLK OUT TO MINIPCIEX1**
CLKOUT_PCIE_N6/CLKOUT_PCIE_P6: AA7 / AA6 — CK_PCIE_PCI6_DN / CK_PCIE_PCI6_DP — **CLK OUT TO PCI BRIDGE**
CLKOUT_PCIE_N7/CLKOUT_PCIE_P7: R6 / R7 — CK_PCIE_1PCIEX1_DN / CK_PCIE_1PCIEX1_DP — **CLK OUT TO PCIEX1**

BT_RADIO_CL R420 10KR2J-3-GP VCC3

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_CLK
Size: C
Document Number: ROSA Shark Bay DTX
Rev: SA
Date: Tuesday, August 06, 2013
Sheet 20 of 52

SATA

25 SATAHDR_RX_DN0
25 SATAHDR_RX_DP0
25 SATAHDR_TX_DN0
25 SATAHDR_TX_DP0

25 SATAHDR_RX_DN1
25 SATAHDR_RX_DP1
25 SATAHDR_TX_DN1
25 SATAHDR_TX_DP1

25 SATAHDR_RX_DN4
25 SATAHDR_RX_DP4
25 SATAHDR_TX_DN4
25 SATAHDR_TX_DP4

25 SATAHDR_RX_DN5
25 SATAHDR_RX_DP5
25 SATAHDR_TX_DN5
25 SATAHDR_TX_DP5

39,45 PCH_SATA_LED_N

Straps

23 SATA1GP
23 SATA2GP
23 SATA3GP

OTHERS

10 H_PM_SYNC_0
10,39 H_PECI
10 H_THERMTRIP_N
12,14,19,39 PWRGD_3V
36 FP_AUD_DETECT
39 A20GATE
39 KBRST_N
39 SER_IRQ
10,14 PLTRST_CPU_N
26 PCIEX16_PRSNT2_N
45 CHASSIS_ID_1
45 CHASSIS_ID_0
22 BOARD_ID_0
42 PCIEX1_PRSNT2_N
45 FP_CBL_DET

HDMI

22,28 DDSP_C_HPD
28 DDPC_CTRL_CLK
28 DDPC_CTRL_DATA

VGA

27 VGA_HSYNC_3V
27 VGA_VSYNC_3V
27 VGA_RED
27 VGA_GREEN
27 VGA_BLUE
27 VGA_PCH_DDCSDA
27 VGA_PCH_DDCSCL

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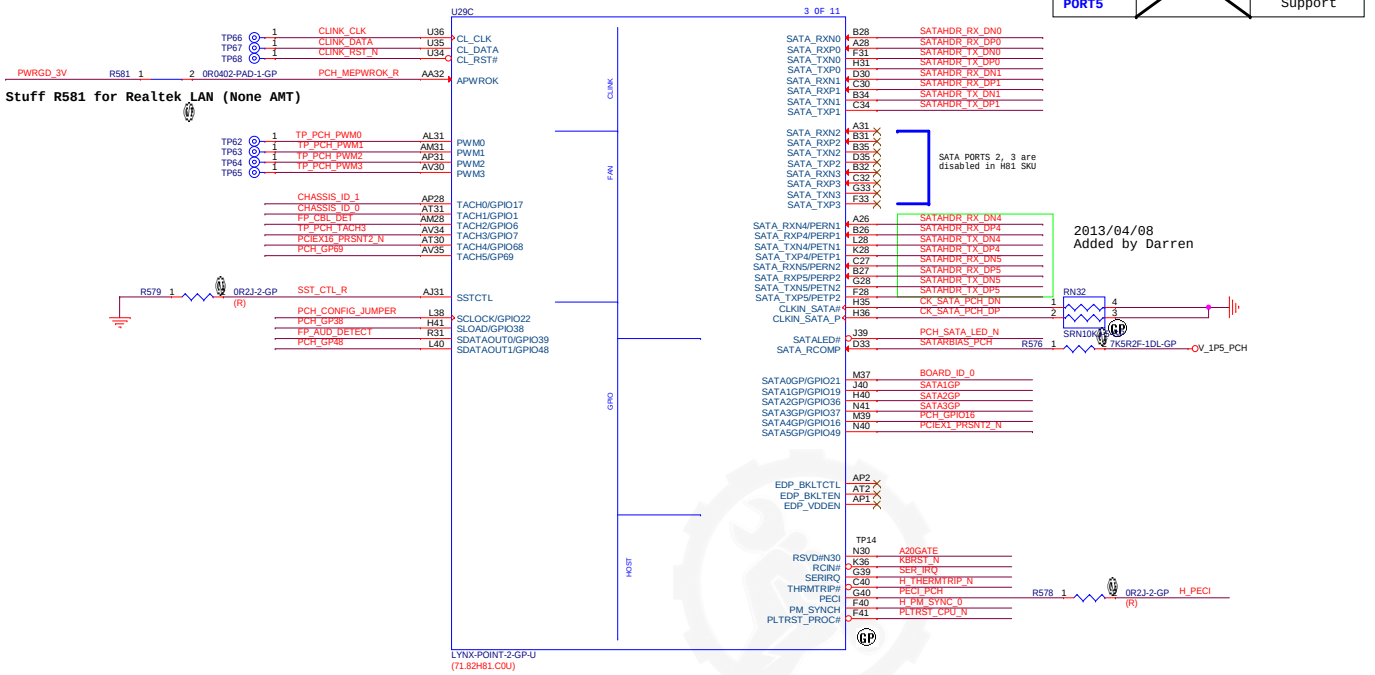
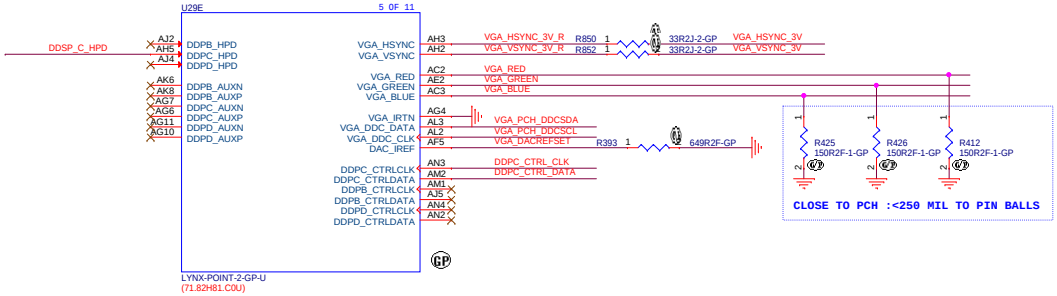
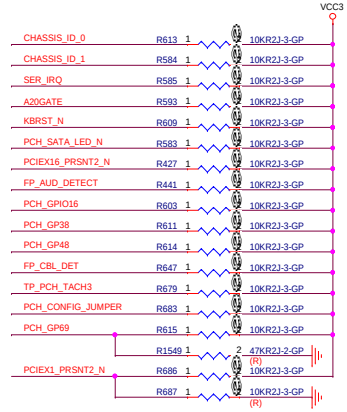
SATA5 Port (H81)

	SATA 3.0 PORT	SATA 2.0 Port
PORT0	Support	Support
PORT1	Support	Support
PORT2		Disabled
PORT3		Disabled
PORT4		Support
PORT5		Support





Pull-up on MB



GPIO49 CAN BE USE AS PCIE/MSATA MUX SELECT IN LPT

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_SATA/FAN/DP/VGA

Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Tuesday, August 06, 2013 | Sheet 21 of 52

DMI

11 DMI_MT_IR_DN[0..3]
11 DMI_MT_IR_DP[0..3]
11 DMI_IT_MR_DN[0..3]
11 DMI_IT_MR_DP[0..3]

PCIE

42 HSI_DN2
42 HSI_DP2
42 HSO_C_DN2
42 HSO_C_DP2

42 HSI_DN3
42 HSI_DP3
42 HSO_C_DN3
42 HSO_C_DP3

35 HSI_DN4
35 HSI_DP4
35 HSO_C_DN4
35 HSO_C_DP4

43 HSI_DN5
43 HSI_DP5
43 HSO_C_DN5
43 HSO_C_DP5

38 HSI_DN6
38 HSI_DP6
38 HSO_C_DN6
38 HSO_C_DP6

USB2.0

33 USB_PCH_DN0
33 USB_PCH_DP0
33 USB_PCH_DN1
33 USB_PCH_DP1
34 USB_PCH_DN2
34 USB_PCH_DP2
34 USB_PCH_DN3
34 USB_PCH_DP3
34 USB_PCH_DN4
34 USB_PCH_DP4
43 USB_PCH_DN5
43 USB_PCH_DP5
31 USB_PCH_DN8
31 USB_PCH_DP8
31 USB_PCH_DN9
31 USB_PCH_DP9
30 USB_PCH_DN10
30 USB_PCH_DP10
30 USB_PCH_DN11
30 USB_PCH_DP11

33 USB_OC_01*
34 USB_OC_23*
34 USB_OC_45*
31 USB_OC_89*
30 USB_OC_1011*

USB3.0

33 USB3_TX0_C_DN
33 USB3_TX0_C_DP
33 USB3_TX1_C_DN
33 USB3_TX1_C_DP
30 USB3_TX2_C_DN
30 USB3_TX2_C_DP

33 USB3_RX0_DN
33 USB3_RX0_DP
33 USB3_RX1_DN
33 USB3_RX1_DP
30 USB3_RX2_DN
30 USB3_RX2_DP

FDI

11 FDI_TX_DN[0..1]
11 FDI_TX_DP[0..1]

11 FDI_INT
11 FDI_CSYNC

OTHERS

20 CK_PCH_33M_FB
43 W1_DETECT_USB
21,28 DDSP_C_HPD
27 VGA_DET

26,39 PLTRST_N
23 P_GNT_N1
23 P_GNT_N2
23 P_GNT_N3
21 BOARD_ID_0
19 BOARD_ID_1
19 BOARD_ID_2

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U29B — LYNX-POINT-2-GP-U (71.82H81.C0U) — 2 OF 11

DMI_MT_IR_DN0 L24 — DMI_RXN0
DMI_MT_IR_DP0 K24 — DMI_RXP0
DMI_IT_MR_DN0 C20 — DMI_TXN0
DMI_IT_MR_DP0 B20 — DMI_TXP0
DMI_MT_IR_DN1 G24 — DMI_RXN1
DMI_MT_IR_DP1 H24 — DMI_RXP1
DMI_IT_MR_DN1 D21 — DMI_TXN1
DMI_IT_MR_DP1 B21 — DMI_TXP1
DMI_MT_IR_DN2 F26 — DMI_RXN2
DMI_MT_IR_DP2 G26 — DMI_RXP2
DMI_IT_MR_DN2 B22 — DMI_TXN2
DMI_IT_MR_DP2 C22 — DMI_TXP2
DMI_MT_IR_DN3 K26 — DMI_RXN3
DMI_MT_IR_DP3 L26 — DMI_RXP3
DMI_IT_MR_DN3 A24 — DMI_TXN3
DMI_IT_MR_DP3 B24 — DMI_TXP3

DMIRCOMP B19 — R697 1 7K5R2F-1DL-GP — R695 1 7K5R2F-1DL-GP — V_1P5_PCH
PCIE_RCOMP C13
100M_DMI_PCH_DN G22
100M_DMI_PCH_DP F22 — RN33 SRN10KJ-5-GP
CLKIN_DMI# — CLKIN_DMI_P

PERN1/USB3RN2 L14
PERP1/USB3RP2 K14
PETN1/USB3TN2 B12
PETP1/USB3TP2 B11
PERN2/USB3RN3 F14
PERP2/USB3RP3 G14
PETN2/USB3TN3 D11
PETP2/USB3TP3 C11
PERN3 F11
PERP3 H11
PETN3 B9
PETP3 A9
PERN4 J11
PERP4 L11
PETN4 B8
PETP4 C8
PERN5 G9
PERP5 F9
PETN5 B7
PETP5 A7
PERN6 F7
PERP6 H7
PETN6 E1
PETP6 D2
PERN7 K6
PERP7 K8
PETN7 G3
PETP7 G5
PERN8 J2
PERP8 J3
PETN8 H2
PETP8 H1

HSI_DN2 — HSO_C_DN2 — C559 1 — C617 1 — SCD1U10V2KX-4GP — HSO_C_DP2 — PCIEX1 CONN
HSI_DP2 — HSO_DN2
HSI_DN3 — HSO_C_DN3 — C159 1 — C160 1 — SCD1U10V2KX-4GP — HSO_C_DP3 — PCIEX1 CONN
HSI_DP3 — HSO_DP2
HSI_DN4 — HSO_C_DN4 — C8 — HSO_C_DP4 — LAN
HSI_DP4 — HSO_DN3
HSI_DN5 — HSO_C_DN5 — C539 1 — C538 1 — SCD1U10V2KX-4GP — HSO_C_DP5 — Mini PCIEX1 SLOT
HSI_DP5 — HSO_DN4
HSI_DN6 — HSO_C_DN6 — (B) C553 1 — (B) C543 1 — SCD1U10V2KX-4GP — HSO_C_DP6 — PCI BRIDGE
HSI_DP6 — HSO_DN5
HSO_DN6
HSO_DP6

PCIE PORTS 7, 8 are disabled in H81 SKU

USB 2.0 PORTS 6, 7 are disabled in H81 SKU
USB 2.0 PORTS 12, 13 are disabled in H81 SKU

USB2N0 AV10 — USB_PCH_DN0 — FOR Rear USB2.0 + USB 3.0
USB2P0 AU10 — USB_PCH_DP0 — FOR Rear USB2.0 + USB 3.0
USB2N1 AV11 — USB_PCH_DN1 — FOR Rear USB 2.0
USB2P1 AU11 — USB_PCH_DP1 — FOR Rear USB 2.0
USB2N2 AN14 — USB_PCH_DN2 — FOR Front USB2.0 header
USB2P2 AP14 — USB_PCH_DP2 — FOR Mini PCIEx1 slot
USB2N3 AJ16 — USB_PCH_DN3
USB2P3 AK16 — USB_PCH_DP3
USB2N4 AU15 — USB_PCH_DN4
USB2P4 AV15 — USB_PCH_DP4
USB2N5 AU12 — USB_PCH_DN5
USB2P5 AT12 — USB_PCH_DP5
USB2N6 AV14
USB2P6 AW14
USB2N7 AU13
USB2P7 AT13
USB2N8 AW16 — USB_PCH_DN8 — FOR Rear USB+LAN
USB2P8 AV16 — USB_PCH_DP8 — FOR Rear USB+LAN
USB2N9 AN16 — USB_PCH_DN9 — FOR Front USB 3.0 header
USB2P9 AP16 — USB_PCH_DP9 — FOR Front USB 3.0 header
USB2N10 AJ18 — USB_PCH_DN10
USB2P10 AK18 — USB_PCH_DP10
USB2N11 AP18 — USB_PCH_DN11
USB2P11 AN18 — USB_PCH_DP11
USB2N12 AW18
USB2P12 AV18
USB2N13 AP20
USB2P13 AN20

GPIO59 AE40 — USB_OC0_R_N — R521 1 — 0R0402-PAD-2-GP — USB_OC_01*
GPIO40 AF37 — USB_OC1_R_N — R496 1 — 0R0402-PAD-2-GP — USB_OC_23*
GPIO41 AD39 — USB_OC2_R_N — R523 1 — 0R0402-PAD-2-GP — USB_OC_45*
GPIO42 AD40 — USB_OC3_R_N
GPIO43 AF39 — USB_OC4_R_N — R493 1 — 2 0R0402-PAD-2-GP — USB_OC_89*
GPIO9 AC41 — USB_OC5_R_N — R483 1 — 2 0R0402-PAD-2-GP — USB_OC_1011*
GPIO10 AF40 — USB_OC6_R_N
GPIO14 AG40 — USB_OC7_R_N

USBRBIAS# AV20 — USBRBIAS_PCH — R617 1 — 22D6R2F-L1-GP — USBRBIAS
CLKIN_DOT96# AP11 — CK_96M_DREF_DN
CLKIN_DOT96_P AM11 — CK_96M_DREF_DP — SRN10KJ-5-GP — RN34

USBRBIAS_PHY (R617): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 1 INCHE TO RESISTOR

SB3V — R621 10KR2J-3-GP — RN36 SRN10KJ-5-GP — (B) R626 10KR2J-3-GP

USB3_RX0_DN — R677 1 — 0R2J-2-GP — USB3_RX0_DN_P
USB3_RX2_DN — R678 1 — 0R2J-2-GP (R) — USB3_RX2_DN
USB3_RX0_DP — R681 1 — 0R2J-2-GP — USB3_RX0_DP_P
USB3_RX2_DP — R689 1 — 0R2J-2-GP (R) — USB3_RX2_DP
USB3_TX0_C_DN — R690 1 — 0R2J-2-GP — USB3_TX0_C_DN_P
USB3_TX2_C_DN — R691 1 — 0R2J-2-GP (R) — USB3_TX2_C_DN
USB3_TX0_C_DP — R692 1 — 0R2J-2-GP — USB3_TX0_C_DP_P
USB3_TX2_C_DP — R699 1 — 0R2J-2-GP (R) — USB3_TX2_C_DP

04/19
Add Co-layout resistors

U29F — LYNX-POINT-2-GP-U (71.82H81.C0U) — 6 OF 11

FOR Front USB 3.0 header and Rear USB3.0 Connector Co-Layout
FOR Rear USB2.0 + USB 3.0

USB3_RX0_DN_P F20 — USB3RN0
USB3_RX0_DP_P G20 — USB3RP0
USB3_TX0_C_DN_P B18 — USB3TN0
USB3_TX0_C_DP_P C18 — USB3TP0
USB3_RX1_DN G18 — USB3RN1
USB3_RX1_DP H18 — USB3RP1
USB3_TX1_C_DN B15 — USB3TN1
USB3_TX1_C_DP B16 — USB3TP1
USB3RN4 K20
USB3RP4 L20
USB3TN4 D15
USB3TP4 C15
USB3RN5 L18
USB3RP5 K18
USB3TN5 B14
USB3TP5 A14

FDI_RXN0 N1 — FDI_TX_DN0
FDI_RXP0 N2 — FDI_TX_DP0
FDI_RXN1 P2 — FDI_TX_DN1
FDI_RXP1 P3 — FDI_TX_DP1
FDI_CSYNC L2 — FDI_CSYNC
FDI_INT L3 — FDI_INT
FDI_RCOMP K2 — FDI_RCOMP — R694 1 — 7K5R2F-1DL-GP — V_1P5_PCH

VCC3 — RN35 SRN10KJ-5-GP — USB 3.0 PORTS 4, 5 are disabled in H81 SKU

PCH_GP70_PU — AK28
PCH_GP71_PU — AT34
TACH6/GPIO70
TACH7/GPIO71

2012/12/12
For Layout, swaping
OLD NET: NET 'USB3_TX1_C_DN' U29.B18
NEW NET: NET 'USB3_TX1_C_DN' U29.G18
OLD NET: NET 'USB3_RX2_DN' U29.G18
NEW NET: NET 'USB3_RX2_DN' U29.B15
OLD NET: NET 'USB3_TX1_C_DP' U29.C18
NEW NET: NET 'USB3_TX1_C_DP' U29.H18
OLD NET: NET 'USB3_RX2_DP' U29.H18
NEW NET: NET 'USB3_RX2_DP' U29.B16
OLD NET: NET 'USB3_TX2_C_DN' U29.B15
NEW NET: NET 'USB3_TX2_C_DN' U29.B18
OLD NET: NET 'USB3_TX2_C_DP' U29.B16
NEW NET: NET 'USB3_TX2_C_DP' U29.C18

BOARD ID

Board	ID0(GPIO21)	ID1(GPIO49)	ID2(GPIO45)
SSI/General	0	0	0
PT/General	0	0	1
ST/General	0	1	0
MP/General	0	1	1
SSI/Great Bear	1	0	0
PT/Great Bear	1	0	1
ST/Great Bear	1	1	0
MP/Great Bear	1	1	1

VCC3 — (B) R651 10KR2J-3-GP — BOARD_ID_0 — R650 10KR2J-3-GP (G)
SB3V — R405 10KR2J-3-GP — BOARD_ID_1 — R403 10KR2J-3-GP (R)
SB3V — (R) R676 10KR2J-3-GP — BOARD_ID_2 — R655 10KR2J-3-GP

U29A — PCI — LYNX-POINT-2-GP-U (71.82H81.C0U) — 1 OF 11

SB3V — R698 1 — (R) 10KR2J-3-GP — P_PME# — CK_PCH_33M_FB
PME# AA31
CLKIN_33MHZLOOPBACK AM22

TP16 A2
TP17 A3
TP18 B2
TP19 B1
TD_IREF C3
R133 1 — 8K2R2F-1-GP — TD_IREF

P_INTA_N AU29 — PIRQA#
P_INTB_N AU27 — PIRQB#
P_INTC_N AW28 — PIRQC#
P_INTD_N AV27 — PIRQD#
W1_DETECT_USB AR30 — GPIO2
DDSP_C_HPD — R599 1 — 1KR2J-1-GP — HDMI_DETECT AV29 — GPIO3
VGA_DET AV28 — GPIO4
P_INTH_N AT27 — GPIO5

PLTRST# AA37 — PLTRST_N
GPIO35_NMI# M40 — PCH_GP35 — TP90
GPIO50 AH26 — P_REQ_N1
GPIO51 AU31 — P_GNT_N1
GPIO52 AJ26 — P_REQ_N2
GPIO53 AV31 — P_GNT_N2
GPIO54 AW33 — P_REQ_N3
GPIO55 R30 — P_GNT_N3

VCC3
P_REQ_N2 — R2250 1 — 8K2R2J-3-GP
P_REQ_N1 — R2251 1 — 8K2R2J-3-GP
W1_DETECT_USB — R2252 1 — 8K2R2J-3-GP
P_REQ_N3 — R2253 1 — 8K2R2J-3-GP
04/23
Change to single resistors

VGA_DET — R596 1 — (R) 10KR2J-3-GP
HDMI_DETECT — R445 1 — (R) 10KR2J-3-GP

RN3
VGA_DET — 1
P_INTH_N — 2
P_INTD_N — 3
P_INTB_N — 4
8 7 6 5
SRN8K2-4-GP

HDMI_DETECT — R2247 1 — (R) 8K2R2J-3-GP
P_INTA_N — R2248 1 — 8K2R2J-3-GP
P_INTC_N — R2249 1 — 8K2R2J-3-GP
04/19
Un-mount HDMI DETECT pull-up resistor

FOR LPT: GP70 STRAP - USB3 PORT4
GP71 - USB3 PORTS
SOFT STRAP TO DETERMINE NATIVE FUNCTION

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_FDI/PCIE/DMI/USB
Size: C
Document Number: ROSA Shark Bay DTX
Rev: SA
Date: Tuesday, August 06, 2013
Sheet 22 of 52

STRAP

21 SATA1GP
21 SATA2GP
21 SATA3GP
22 P_GNT_N1

10 HSW_STRAP_13
19 IGC_EN_N

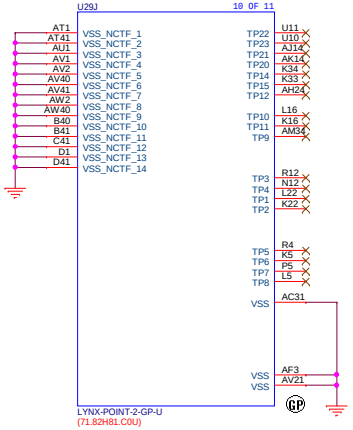
19 AUD_LINK_SDO_R
19 SUSCLK
19,36 SPKR

22 P_GNT_N2
22 P_GNT_N3

19 PCH_INTVRMEN

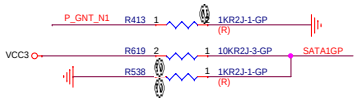
19 DSWVRMEN

19 PCH_GP15

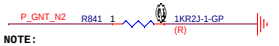


BOOT SELECT STRAPS

BOOT DEVICE	GNT1/ GPIO51	SATA16P /GPIO19
LPC	0	0
SPI	1	1



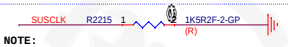
DESIGN NOTE:
WEAK INTERNAL PULLUPS ON GP51. DEFAULT SPI BOOT DEVICE.



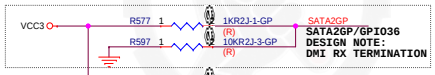
DESIGN NOTE:
FULL VOLTAGE MODE WHEN SAMPLED LOW
DMI AC COUPLING

DESIGN NOTE:
A16 SWAP OVERRIDE OVERRIDE IF SAMPLED LOW

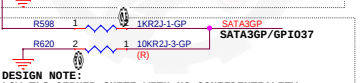
DESIGN NOTE:
SPI OVERRIDE PROTECTION



DESIGN NOTE:
OD PLL VR ENABLE
DISABLE WHEN SAMPLED LOW

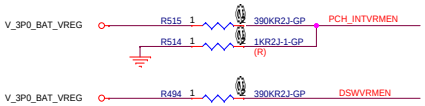


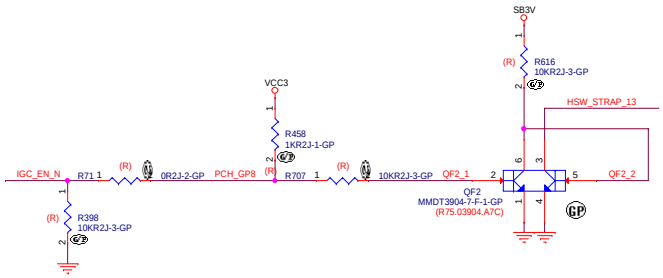
SATA2GP/GPIO36
DESIGN NOTE:
DMI RX TERMINATION



SATA3GP/GPIO37

DESIGN NOTE:
LOW:TLS CIPHER SUITE WITH NO CONFIDENTIALITY.
HIGH:TLS CIPHER SUITE WITH CONFIDENTIALITY.





PCH Functional Straps

PCH EDS,Page88,Table 2-27

SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot"mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3VB	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
PCH_INTVRMEN	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal pull-ups.
SATA1GP (GPIO19)	Boot BIOS Destination Selection Signal has weak internal pull-ups.
P_GNT_N2	The signal has a weak internal pull-up.
AUD_LINK_SDO_R	Flash Descriptor Security Override Strap .
AUD_LINK_SYNC-R	The signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
PCH_GP28_PU (GPIO28) USB_CH_M2	The signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
DF_TVS	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal pull-down.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
CDC_DWN_DISABLE (SATA2GP/GPIO36)	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
PCH_GP37 (SATA3GP/GPIO37)	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
TLS_EN (GPIO15)	The signal has a weak internal pull-down. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality A strong pull up may be needed for GPIO functionality

<Variant Name>

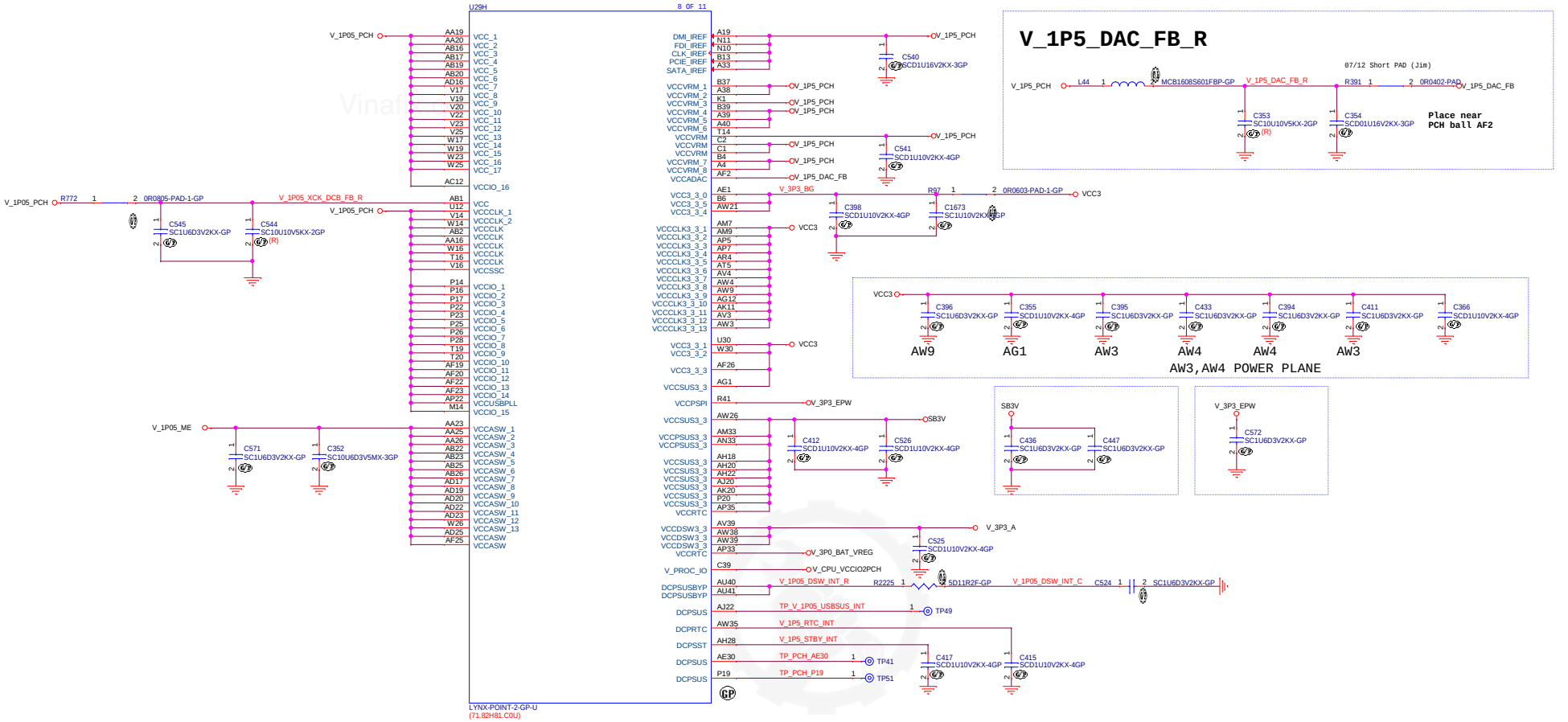
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_GND/STRAPS

Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Tuesday, August 06, 2013 | Sheet 23 of 52



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_POWER

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Tuesday, August 06, 2013 Sheet 24 of 52

SATA

21 SATAHDR_RX_DP0
21 SATAHDR_RX_DN0

21 SATAHDR_TX_DN0
21 SATAHDR_TX_DP0

21 SATAHDR_RX_DP1
21 SATAHDR_RX_DN1

21 SATAHDR_TX_DN1
21 SATAHDR_TX_DP1

21 SATAHDR_RX_DP4
21 SATAHDR_RX_DN4

21 SATAHDR_TX_DN4
21 SATAHDR_TX_DP4

21 SATAHDR_RX_DP5
21 SATAHDR_RX_DN5

21 SATAHDR_TX_DN5
21 SATAHDR_TX_DP5

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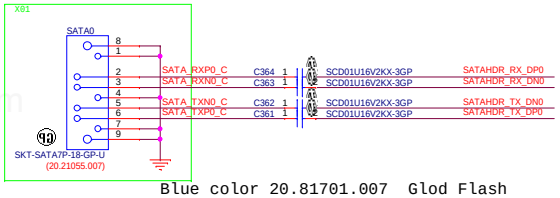
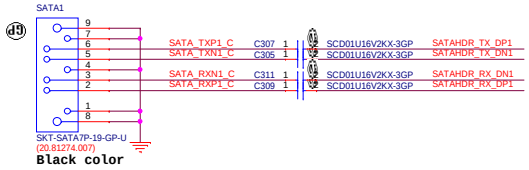
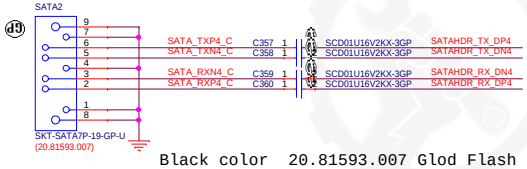


Blue color 20.81701.007 Glod Flash
Pin length 2.1mm

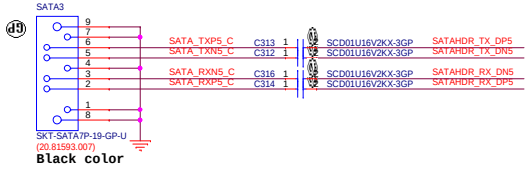


Black color

White color 20.81274.007 15u"
Pin length 2.05mm



Black color 20.81593.007 Glod Flash
Pin length 2.10mm



Black color

Black 20.81593.007 Glod Flash
Pin length 2.10mm

2013/04/08
Added by Darren

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SATA Port

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Monday, August 05, 2013 Sheet 25 of 52

w/o Latch: 20.50352.164
with Latch: 20.50356.164

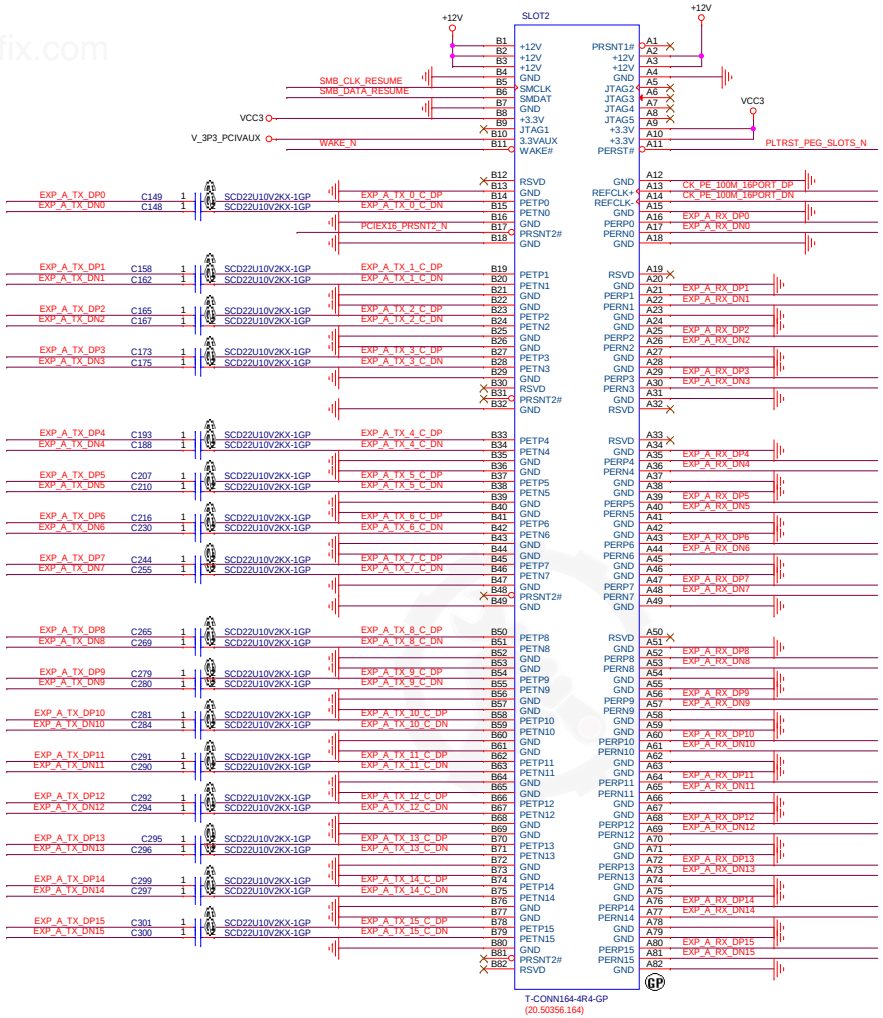
PCIEx16 CONN may need LATCH if supporting 75W GFX Card

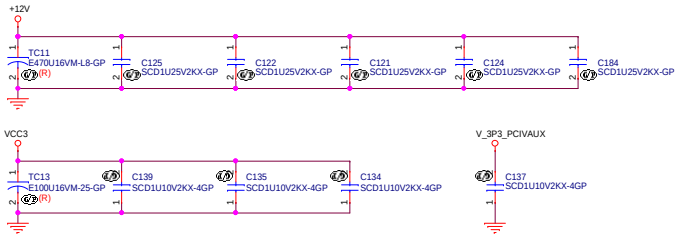
PCIEX16

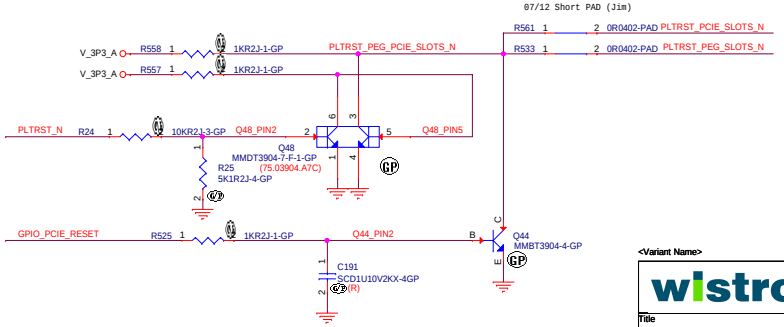
11 EXP_A_RX_DN[0..15]
11 EXP_A_RX_DP[0..15]
11 EXP_A_TX_DP[0..15]
11 EXP_A_TX_DN[0..15]
20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN

OTHERS

19,39,42,43,44 SMB_CLK_RESUME
19,39,42,43,44 SMB_DATA_RESUME
19,35,38,42,43 WAKE_N
21 PCIEX16_PRSNT2_N
22,39 PLTRST_N
19 GPIO_PCIE_RESET
42,43 PLTRST_PCIE_SLOTS_N







<Variant Name>

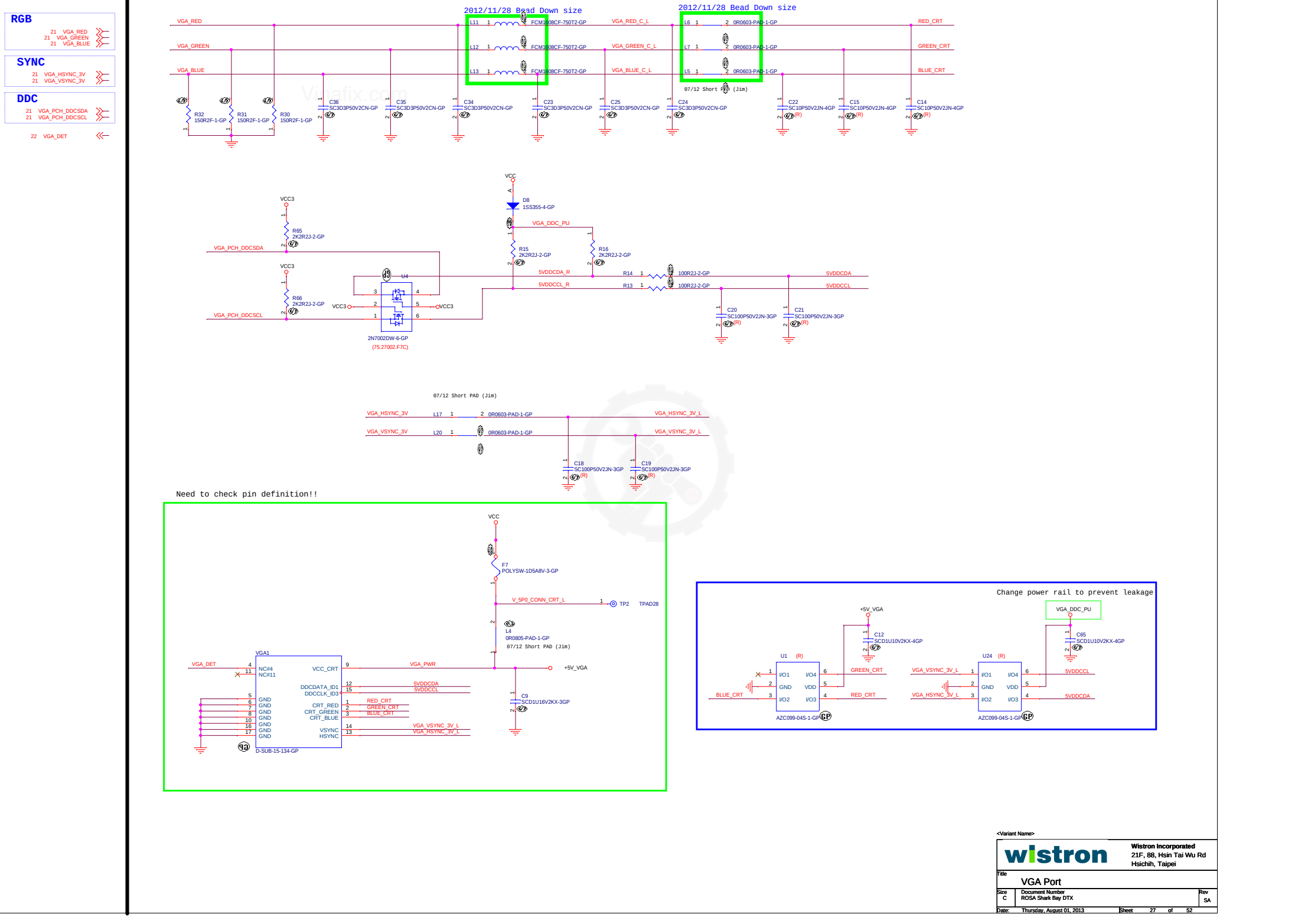
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCIEX16 CONNECTOR

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 26 of 52



<Variant Name>

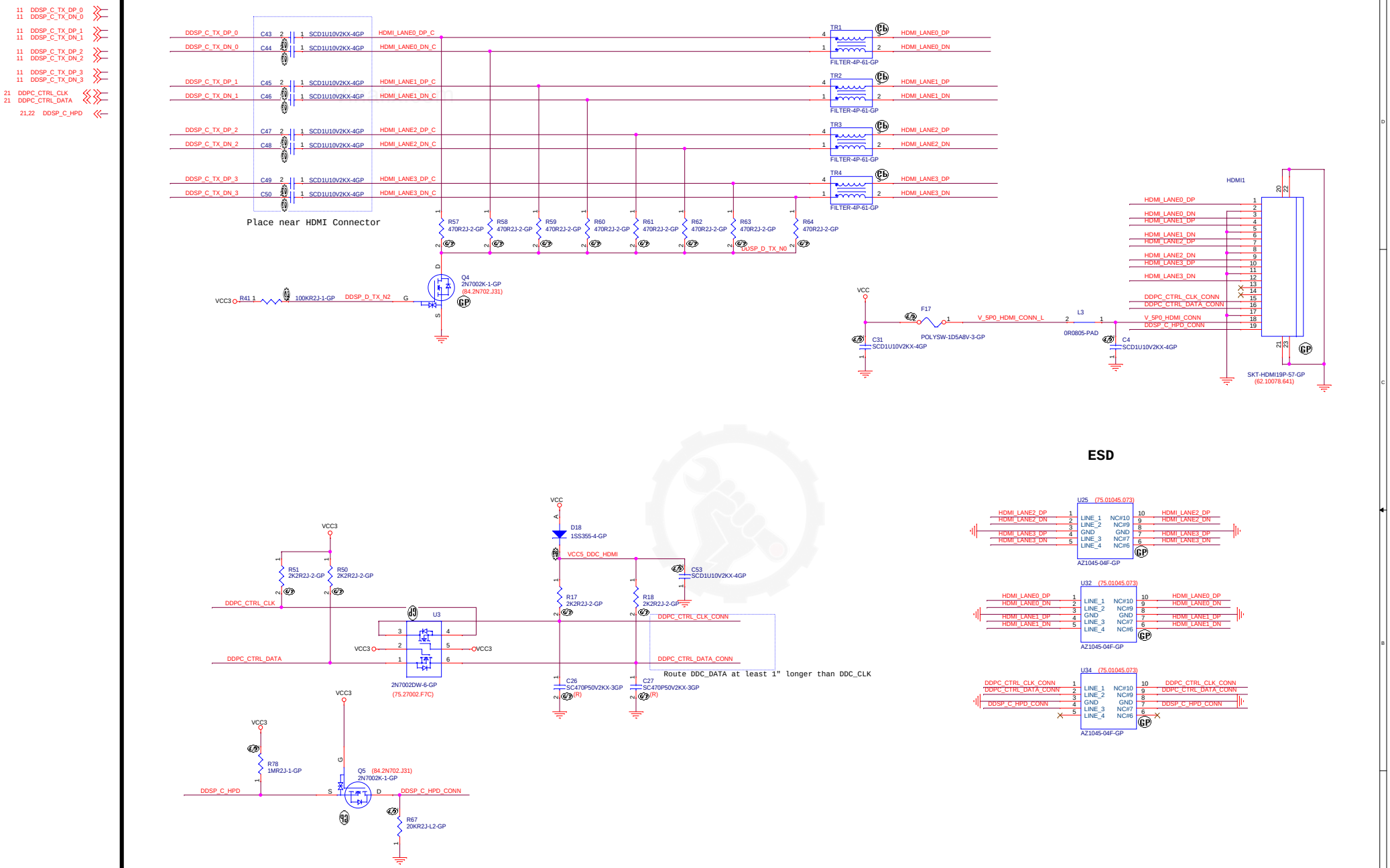
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA Port

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 27 of 52



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDMI Port

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 28 of 52

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<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

Display Port(Taken)

Size	Document Number	Rev
A	ROSA Shark Bay DTX	SA

Date:	Thursday, August 01, 2013	Sheet 29 of 52

FRONT USB

22 USB_PCH_DP10
22 USB_PCH_DN10
22 USB_PCH_DP11
22 USB_PCH_DN11

22 USB_OC_1011*

19 FB_USBF2_DET

22 USB3_RX2_DN
22 USB3_RX2_DP
22 USB3_TX2_C_DN
22 USB3_TX2_C_DP

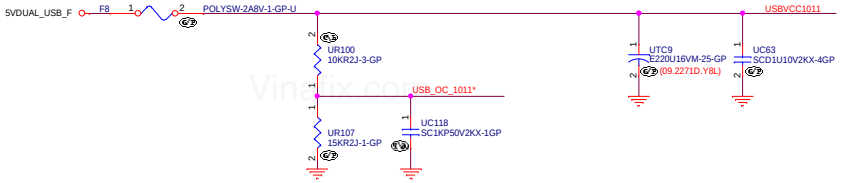
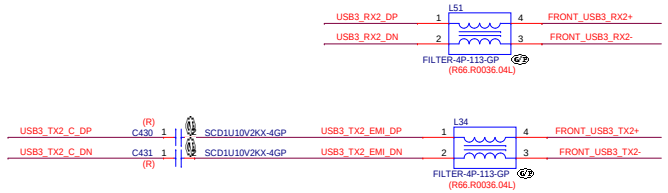
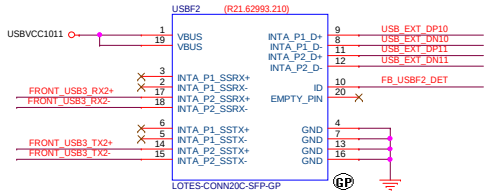


Table 2-1: USB3 ICC A Pin Assignment and Description

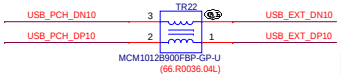
Pin No.	Signal	Description
1	Vbus	Power
2	IntA_P1_SSRX-	USB3 ICC Port1 SuperSpeed Rx-
3	IntA_P1_SSRX+	USB3 ICC Port1 SuperSpeed Rx+
4	GND	GND
5	IntA_P1_SSTX-	USB3 ICC Port1 SuperSpeed Tx-
6	IntA_P1_SSTX+	USB3 ICC Port1 SuperSpeed Tx+
7	GND	GND
8	IntA_P1_D-	USB3 ICC Port1 D- (USB2 Signal D-)
9	IntA_P1_D+	USB3 ICC Port1 D+ (USB2 Signal D+)
10	ID	Over Current Protection
11	IntA_P2_D+	USB3 ICC Port2 D+ (USB2 Signal D+)
12	IntA_P2_D-	USB3 ICC Port2 D- (USB2 Signal D-)
13	GND	GND
14	IntA_P2_SSTX+	USB3 ICC Port2 SuperSpeed Tx+
15	IntA_P2_SSTX-	USB3 ICC Port2 Super Speed Tx-
16	GND	GND
17	IntA_P2_SSRX+	USB3 ICC Port2 SuperSpeed Rx+
18	IntA_P2_SSRX-	USB3 ICC Port2 SuperSpeed Rx-
19	Vbus	Power

USB 3.0

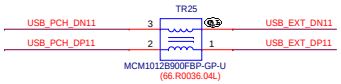


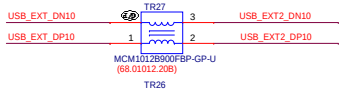


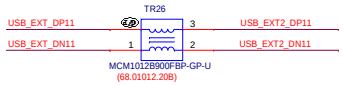
USB 2.0



USBF2 (Default 0 ohm)



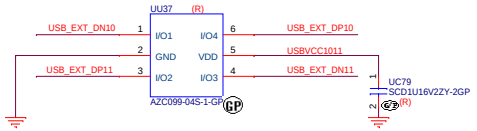




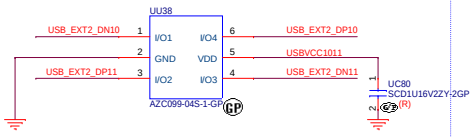
USBF2 (Default Comoon choke)

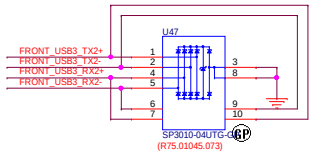
ESD

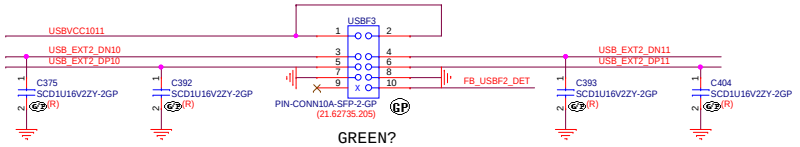
USBF2



USBF3







GREEN?

For Front USB2.0

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FRONT USB2.0 HEADER

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 30 of 52

REAR USB+LAN

22 USB_PCH_DN8
22 USB_PCH_DP8
22 USB_PCH_DN9
22 USB_PCH_DP9

35 LAN_MDI2_DP
35 LAN_MDI2_DN
35 LAN_MDI1_DP
35 LAN_MDI1_DN
35 LAN_MDI0_DP
35 LAN_MDI0_DN
35 LAN_MDI3_DP
35 LAN_MDI3_DN

35 SPEED_100_N
35 SPEED_1000_N
31,35 LINK_ACTIVITY_N

22 USB_OC_89*

5VDUAL_USB_R — F18 — POLYSW-1D5A8V-3-GP — USBVCC89

UTC5 E220U16VM-25-GP (09.2271D.Y8L)
UC22 SCD1U10V2KX-4GP
UR118 10KR2J-3-GP
USB_OC_89*
UR119 15KR2J-1-GP
UC133 SC1KP50V2KX-1GP

USB+RJ45

RJ45
Orange
Green
SPEED_1000 — UR108 249R2F-GP — SPEED_1000_N
SPEED_100 — UR109 249R2F-GP — SPEED_100_N
USBVCC89
USB_EXT_DN9
USB_EXT_DN8
USB_EXT_DP9
USB_EXT_DP8
UP
LAN_MDI3_DN_C
LAN_MDI3_DP_C
LAN_MDI2_DN_C
LAN_MDI2_DP_C
LAN_MDI1_DN_C
LAN_MDI1_DP_C
LAN_MDI0_DN_C
LAN_MDI0_DP_C
LAN_CONN_CVT
RJ45_ACT
OV_3P3_LAN
LINK_ACTIVITY — UR112 330R2J-3-GP
UC103 SC1U10V3KX-3GP (R)
UC104 SCD1U10V2KX-4GP
LINK_ACTIVITY_N
SKT-RJ45-USB-9-GP

TR9 MCM1012B900FBP-GP-U (68.01012.20B)
TR10 MCM1012B900FBP-GP-U (68.01012.20B)
UU12 AZC099-04S-1-GP
UC132 SCD1U16V2ZY-2GP (R)

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

TR14 MCM1012B900FBP-GP-U (66.R0036.04L)
TR12 MCM1012B900FBP-GP-U (66.R0036.04L)
TR13 MCM1012B900FBP-GP-U (66.R0036.04L)
TR11 MCM1012B900FBP-GP-U (66.R0036.04L)

Jim Modify 0816
75.01215.07C
75.00005.D7C
075.003V3.007C

U6 AZC099-04S-1-GP (75.01215.07C)
C3326 SCD1U16V2KX-3GP
U9 AZC099-04S-1-GP (75.01215.07C)
C3327 SCD1U16V2KX-3GP
U11 AZC099-04S-1-GP (75.01215.07C)
C3328 SCD1U16V2KX-3GP

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

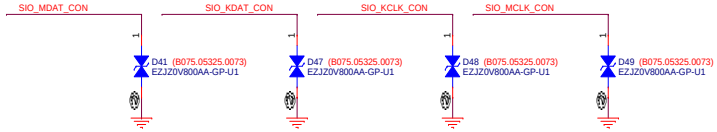
Title: USB+RJ45
Size: C
Document Number: ROSA Shark Bay DTX
Rev: SA
Date: Friday, August 16, 2013
Sheet 31 of 52

Vinafix.com

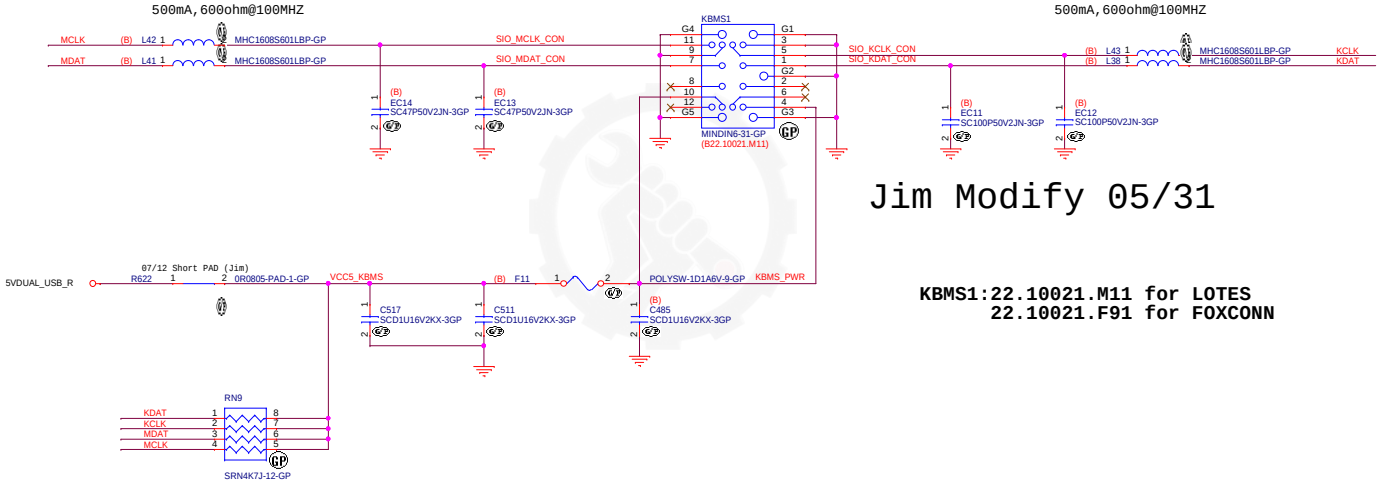
KBMS

39 KCLK
39 KDAT
39 MCLK
39 MDAT

Jason Modify 06/22



KB/MS INTERFACE



Jim Modify 05/31

KBMS1:22.10021.M11 for LOTES
22.10021.F91 for FOXCONN

<Variant Name>

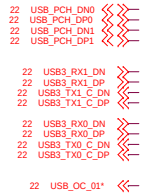
wistron

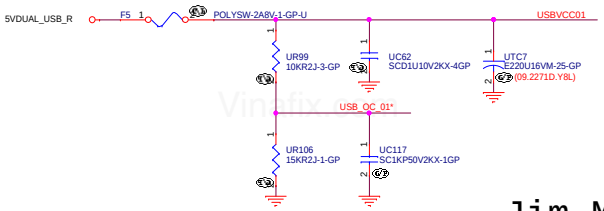
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: KBMS

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

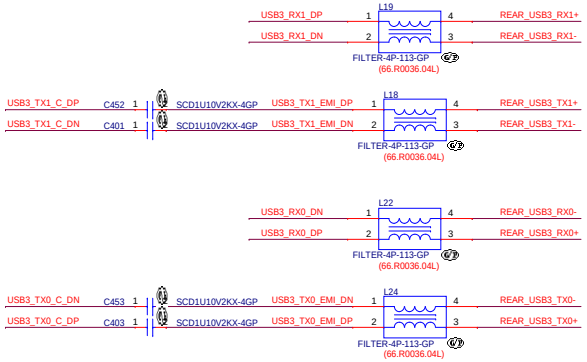
Date: Wednesday, August 07, 2013 Sheet 32 of 52



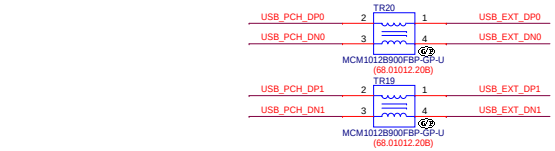


Jim Modify 05/31

USB 3.0

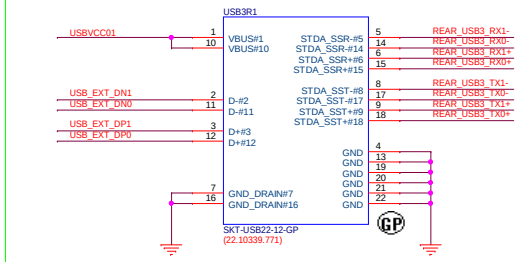


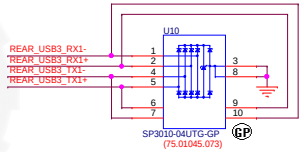
USB 2.0

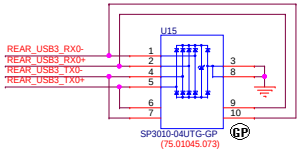


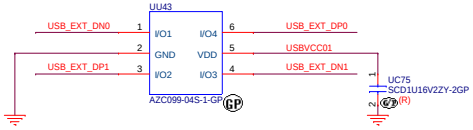
2013/04/19
Modified by Darren

REAR USB3.0 CONN









<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

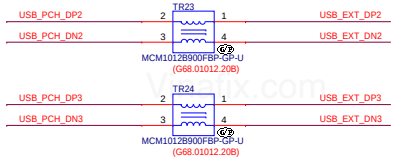
Title: REAR USB3.0

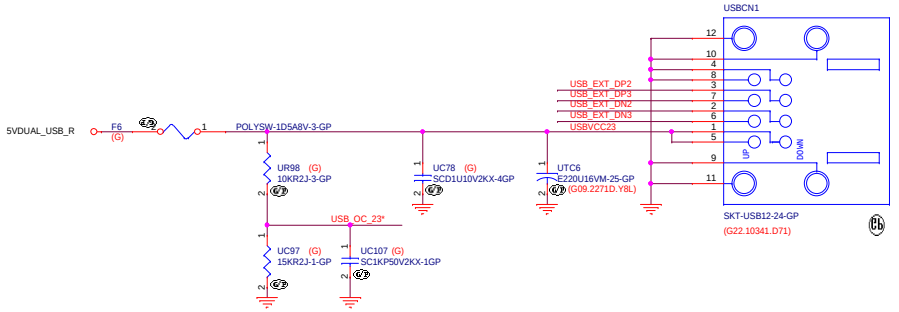
Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 33 of 52

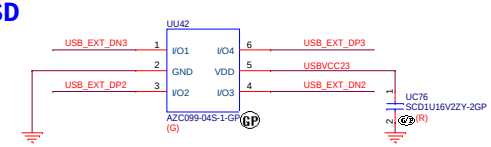
22 USB_PCH_DP2
22 USB_PCH_DN2
22 USB_PCH_DP3
22 USB_PCH_DN3
22 USB_PCH_DN4
22 USB_PCH_DP4
22 USB_OC_23*
22 USB_OC_45*
19 FB_USBFI_DET

Rear USB 2.0

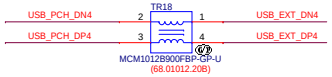


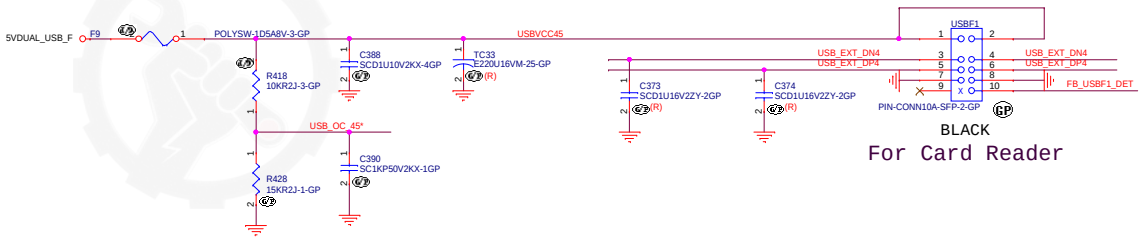


ESD

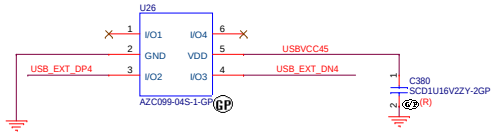


FRONT USB PORT





ESD



<Variant Name>

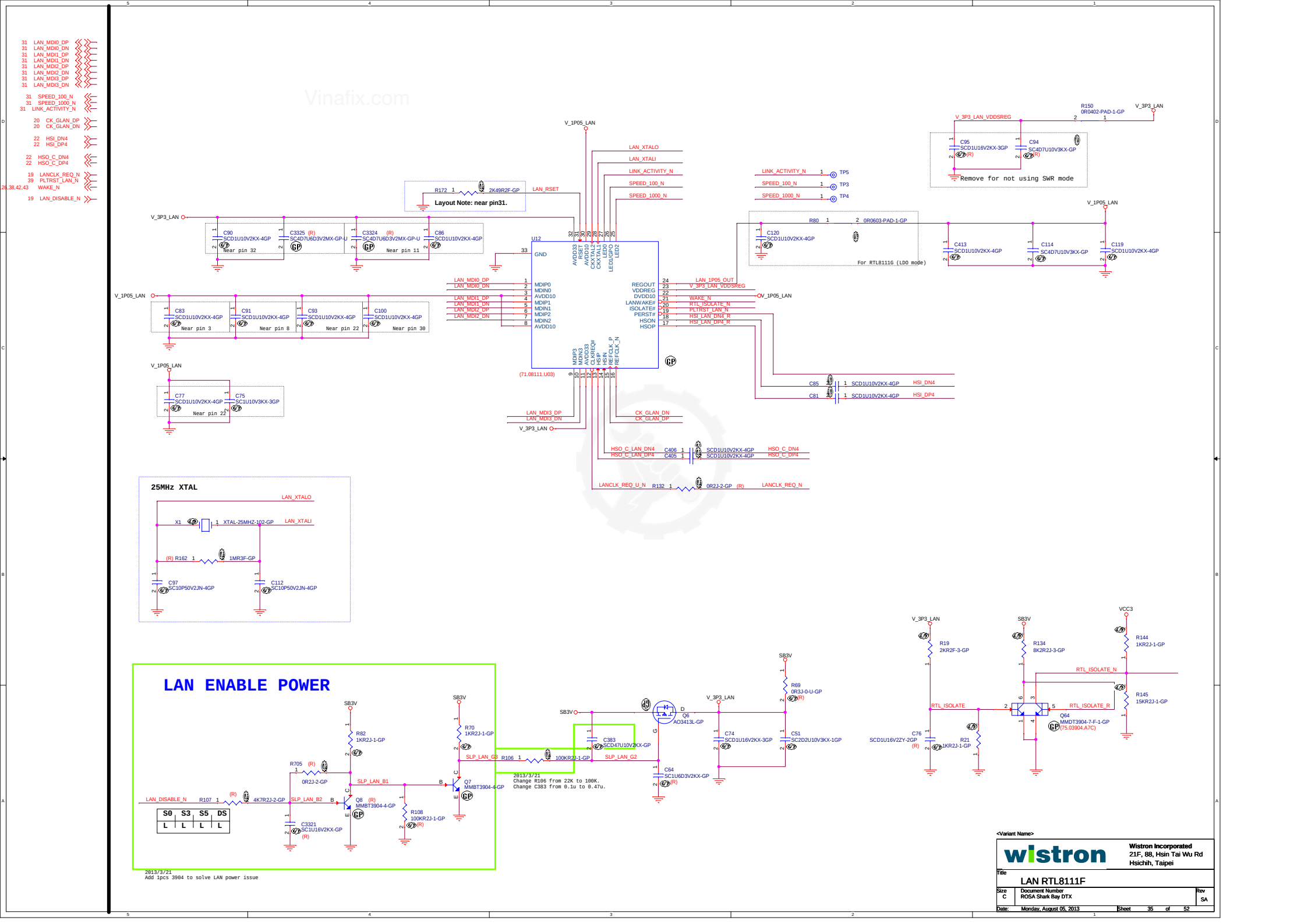
wistron

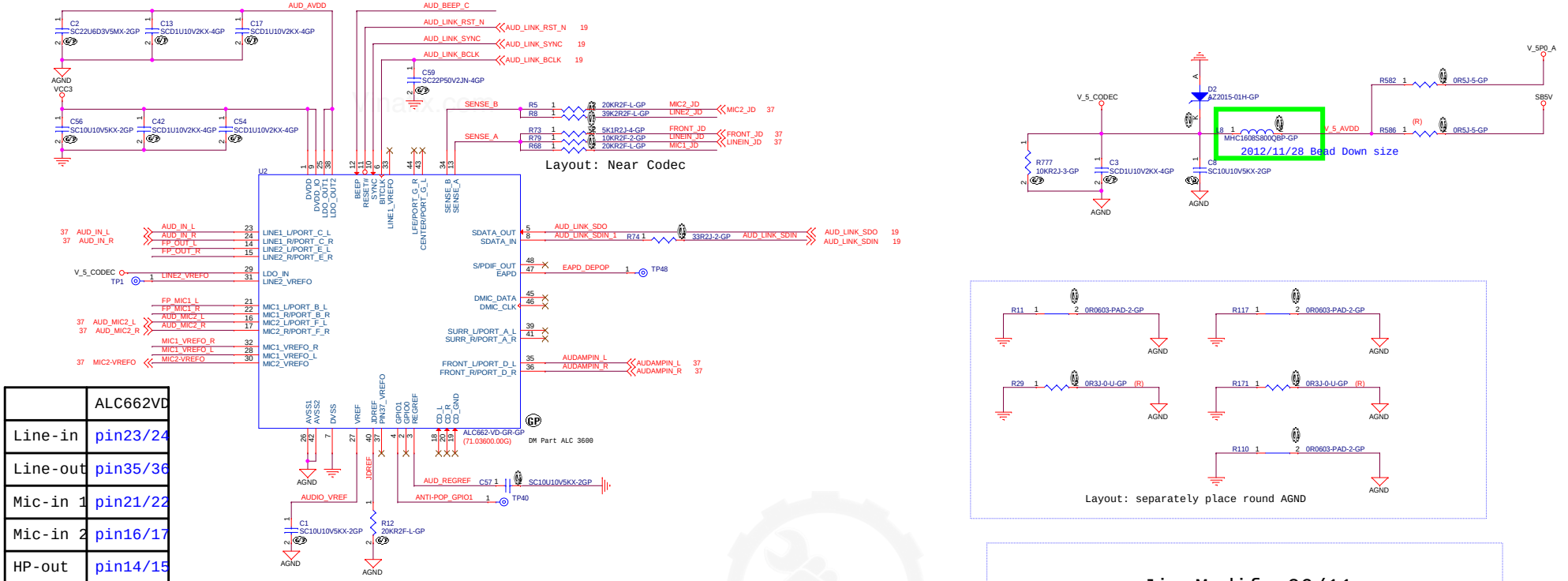
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB2.0

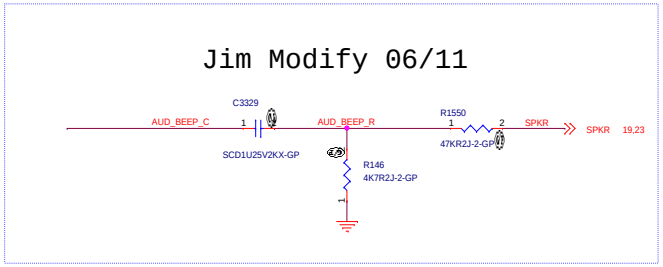
Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Tuesday, August 06, 2013 Sheet 34 of 52

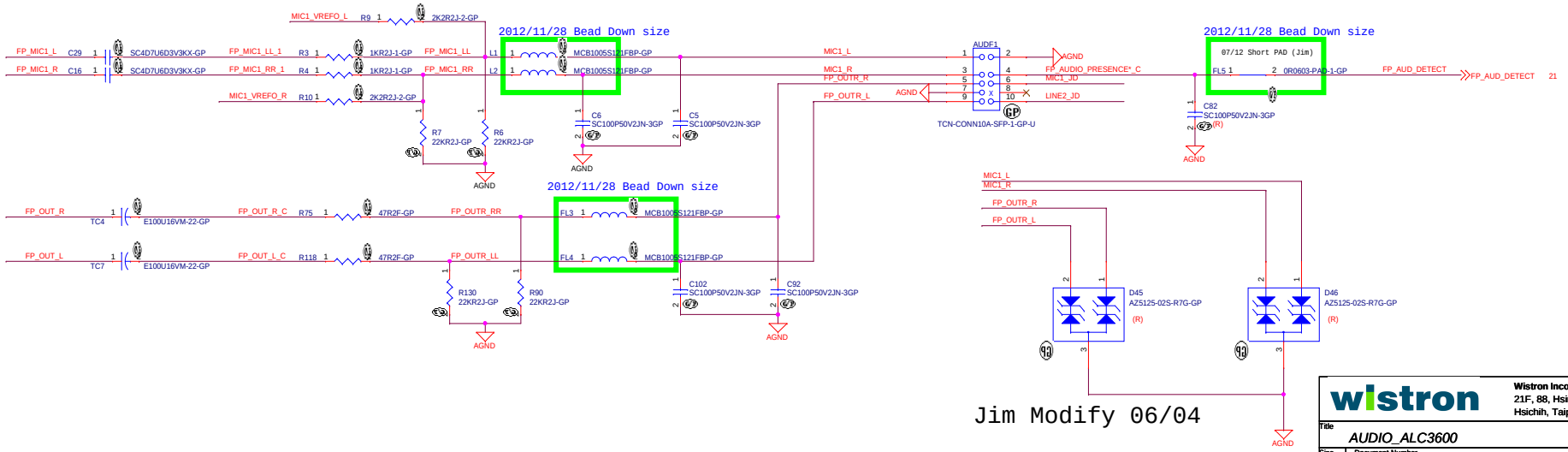

LAN_MDI0_DP
LAN_MDI0_DN
LAN_MDI1_DP
LAN_MDI1_DN
LAN_MDI2_DP
LAN_MDI2_DN
LAN_MDI3_DP
LAN_MDI3_DN
SPEED_100_N
SPEED_1000_N
LINK_ACTIVITY_N
CK_GLAN_DP
CK_GLAN_DN
HSI_DN4
HSI_DP4
HSO_C_DN4
HSO_C_DP4
LANCLK_REQ_N
PLTRST_LAN_N
WAKE_N
LAN_DISABLE_N
Vinafix.com
V_1P05_LAN
V_3P3_LAN
LAN_XTALO
LAN_XTALI
LINK_ACTIVITY_N
SPEED_100_N
SPEED_1000_N
R172 2K49R2F-GP
LAN_RSET
Layout Note: near pin31.
U12
GND
AVDD33
RSET
AVDD10
CKXTAL2
CKXTAL1
LED0
LED1/EE
LED2
MDIP0
MDIN0
AVDD10
MDIP1
MDIN1
MDIP2
MDIN2
AVDD10
REGOUT
VDDREG
DVDD10
LANWAKE#
ISOLATE#
PERST#
HSON
HSOP
MDIP3
MDIN3
AVDD33
CLKREQ#
HSIP
HSIN
REFCLK_P
REFCLK_N
LAN_1P05_OUT
V_3P3_LAN_VDDSREG
WAKE_N
RTL_ISOLATE_N
PLTRST_LAN_N
HSI_LAN_DN4_R
HSI_LAN_DP4_R
(71.08111.U03)
C90 SCD1U10V2KX-4GP Near pin 32
C3325 (R) SC4D7U6D3V2MX-GP-U
C3324 (R) SC4D7U6D3V2MX-GP-U Near pin 11
C86 SCD1U10V2KX-4GP
C83 SCD1U10V2KX-4GP Near pin 3
C91 SCD1U10V2KX-4GP Near pin 8
C93 SCD1U10V2KX-4GP Near pin 22
C100 SCD1U10V2KX-4GP Near pin 30
C77 SCD1U10V2KX-4GP Near pin 22
C75 SC1U10V3KX-3GP
R80 0R0603-PAD-1-GP
For RTL8111G (LDO mode)
C120 SCD1U10V2KX-4GP
C413 SCD1U10V2KX-4GP
C114 SC4D7U10V3KX-GP
C119 SCD1U10V2KX-4GP
R150 0R0402-PAD-1-GP
V_3P3_LAN_VDDSREG
C95 SCD1U16V2KX-3GP (R)
C94 SC4D7U10V3KX-GP (R)
Remove for not using SWR mode
TP5
TP3
TP4
C85 SCD1U10V2KX-4GP HSI_DN4
C81 SCD1U10V2KX-4GP HSI_DP4
C406 SCD1U10V2KX-4GP HSO_C_DN4
C405 SCD1U10V2KX-4GP HSO_C_DP4
LANCLK_REQ_U_N R132 0R2J-2-GP (R) LANCLK_REQ_N
25MHz XTAL
X1 XTAL-25MHZ-102-GP
(R) R162 1MR3F-GP
C97 SC10P50V2JN-4GP
C112 SC10P50V2JN-4GP
LAN ENABLE POWER
SB3V
R82 1KR2J-1-GP
R705 (R) 0R2J-2-GP
SLP_LAN_B1
SLP_LAN_B2
LAN_DISABLE_N
R107 (R) 4K7R2J-2-GP
Q8 (R) MMBT3904-4-GP
C3321 SC1U16V2KX-GP (R)
R108 100KR2J-1-GP (R)
R70 1KR2J-1-GP
SLP_LAN_G3
Q7 MMBT3904-4-GP
R106 100KR2J-1-GP
SLP_LAN_G2
C383 SCD47U10V2KX-GP
Q6 AO3413L-GP
C64 SC1U6D3V2KX-GP (R)
C74 SCD1U16V2KX-3GP
C51 SC2D2U10V3KX-1GP
R69 0R3J-0-U-GP (R)
S0 S3 S5 DS
L L L L
2013/3/21
Change R106 from 22K to 100K.
Change C383 from 0.1u to 0.47u.
2013/3/21
Add 1pcs 3904 to solve LAN power issue
VCC3
R19 2KR2F-3-GP
R134 8K2R2J-3-GP
R144 1KR2J-1-GP
R145 15KR2J-1-GP
RTL_ISOLATE_N
RTL_ISOLATE
RTL_ISOLATE_R
Q64 MMDT3904-7-F-1-GP (75.03904.A7C)
C76 SCD1U16V2ZY-2GP (R)
R21 1KR2J-1-GP
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
LAN RTL8111F
Size C
Document Number ROSA Shark Bay DTX
Rev SA
Date: Monday, August 05, 2013
Sheet 35 of 52



	ALC662VD
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
HP-out	pin14/15



Front Panel



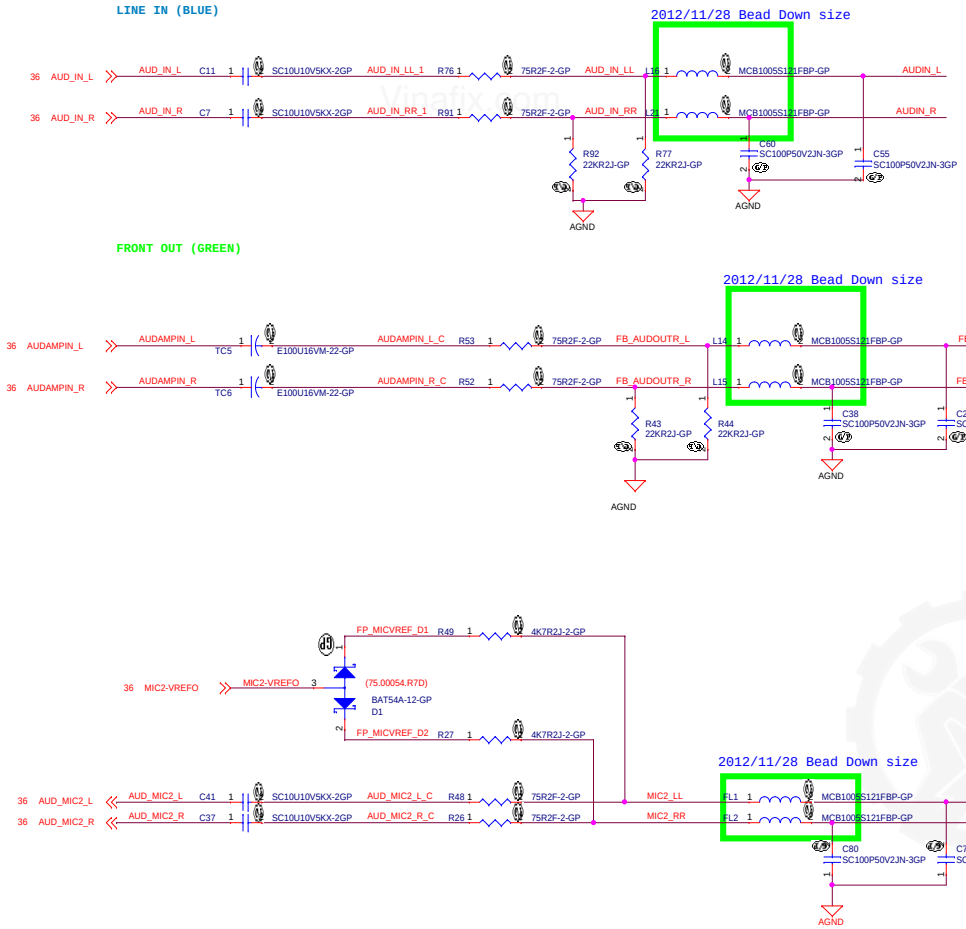
wistron

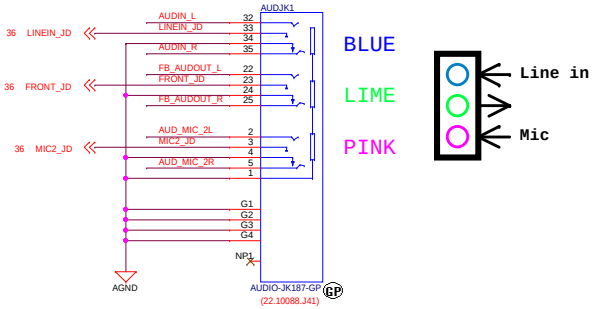
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

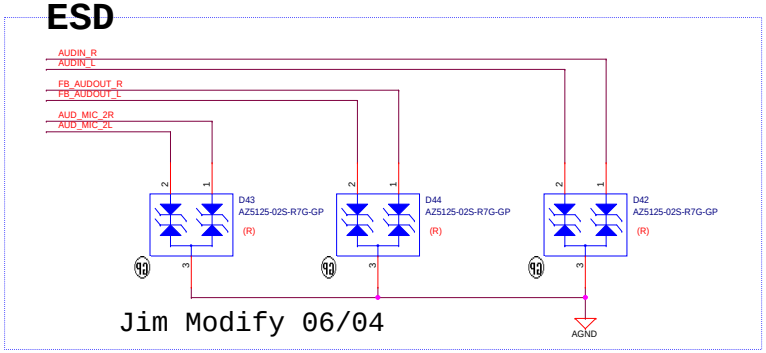
Title: AUDIO_ALC3600

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 36 of 52







<variant_name>

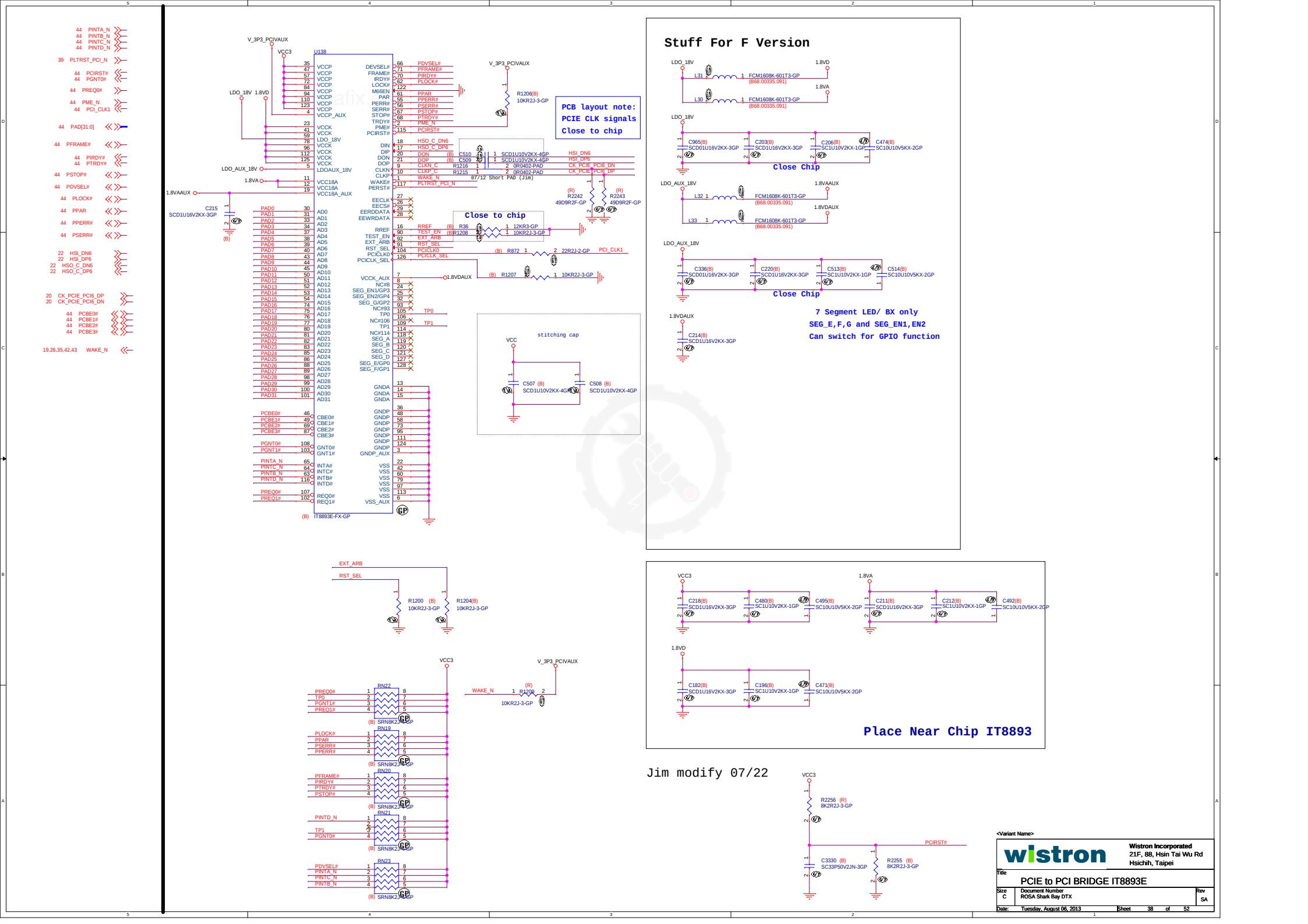
wistron

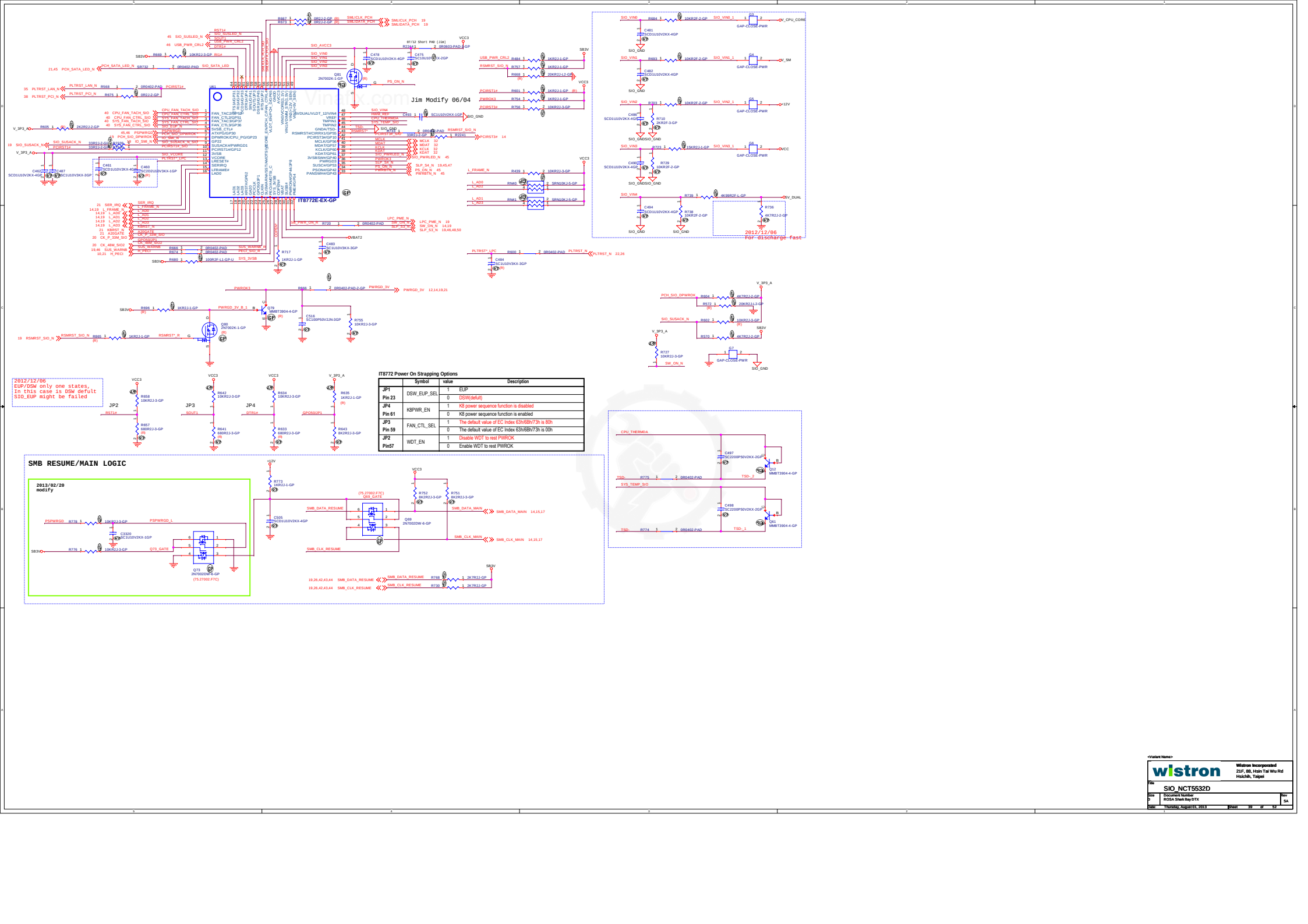
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO_JACKS

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Tuesday, August 06, 2013 Sheet 37 of 52


Stuff For F Version
PCB layout note:
PCIE CLK signals
Close to chip
Close Chip
7 Segment LED/ BX only
SEG_E,F,G and SEG_EN1,EN2
Can switch for GPIO function
Place Near Chip IT8893
Jim modify 07/22
IT8893E-FX-GP
stitching cap
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
PCIE to PCI BRIDGE IT8893E
Document Number
ROSA Shark Bay DTX
Tuesday, August 06, 2013
Sheet 38 of 52



	Symbol	value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin 23		0	DSW(defult)
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 61		0	K8 power sequence function is enabled
JP3	FAN_CTL_SEL	1	The default value of EC Index 63h/6Bh/73h is 80h
Pin 59		0	The default value of EC Index 63h/6Bh/73h is 00h
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin57		0	Enable WDT to rest PWROK

<Variant Name>

wistron

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21F, 88, Hsin Tai Wu Rd
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Title: SIO_NCT5532D

Size: D | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Thursday, August 01, 2013 | Sheet 39 of 52

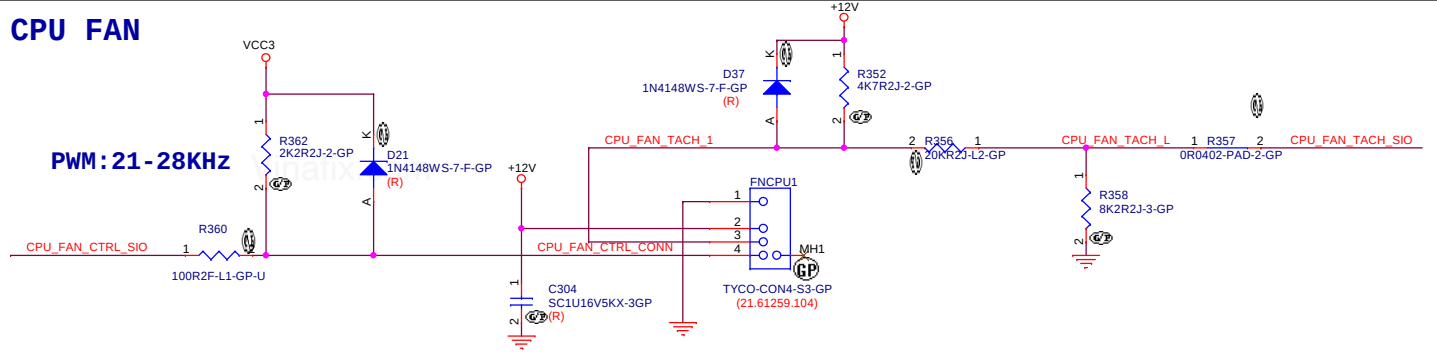
SIO FAN CONTROL

39 CPU_FAN_CTRL_SIO
39 CPU_FAN_TACH_SIO

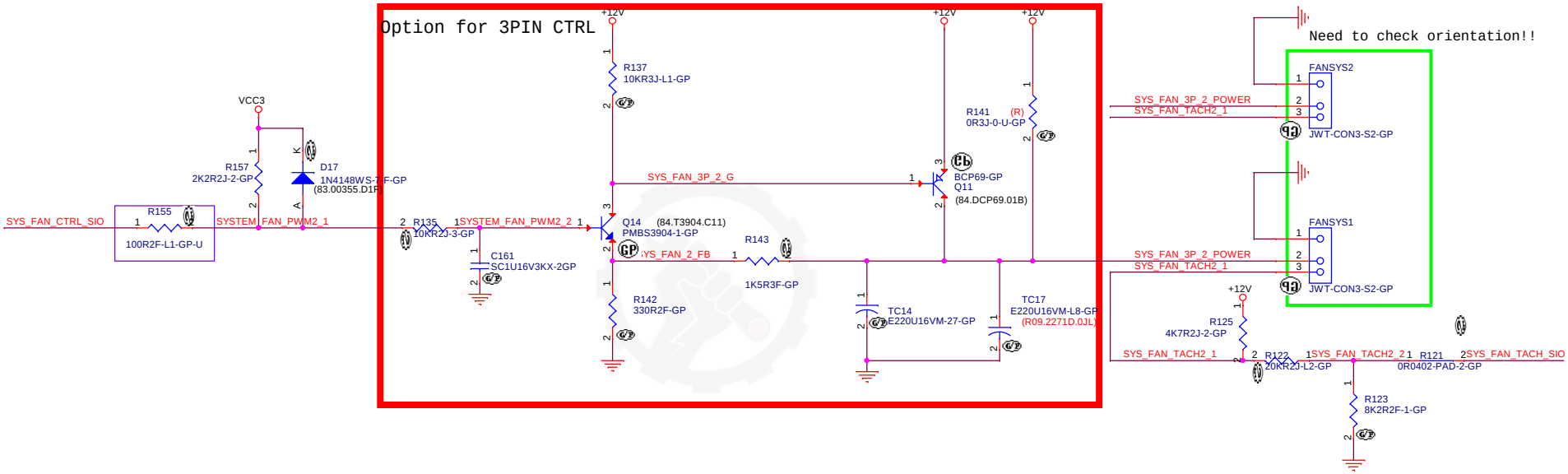
39 SYS_FAN_CTRL_SIO
39 SYS_FAN_TACH_SIO

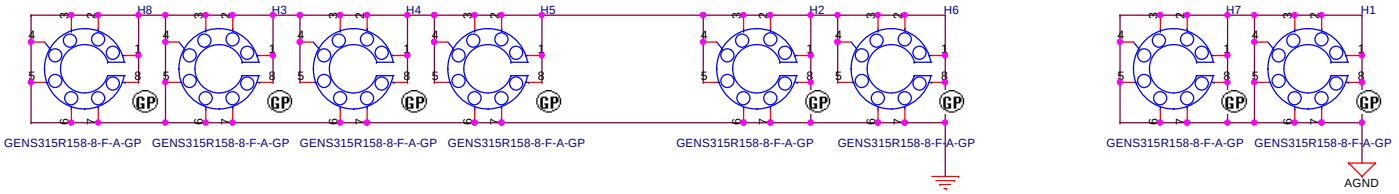
CPU FAN

PWM:21-28KHz



MT and ST SYS 3 PINS/4 PINS FAN CONTROL





<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FAN CIRCUITS/HOLE

Size	Document Number	Rev
Custom	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 40 of 52

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<Variant Name>

wistron

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Hsichih, Taipei

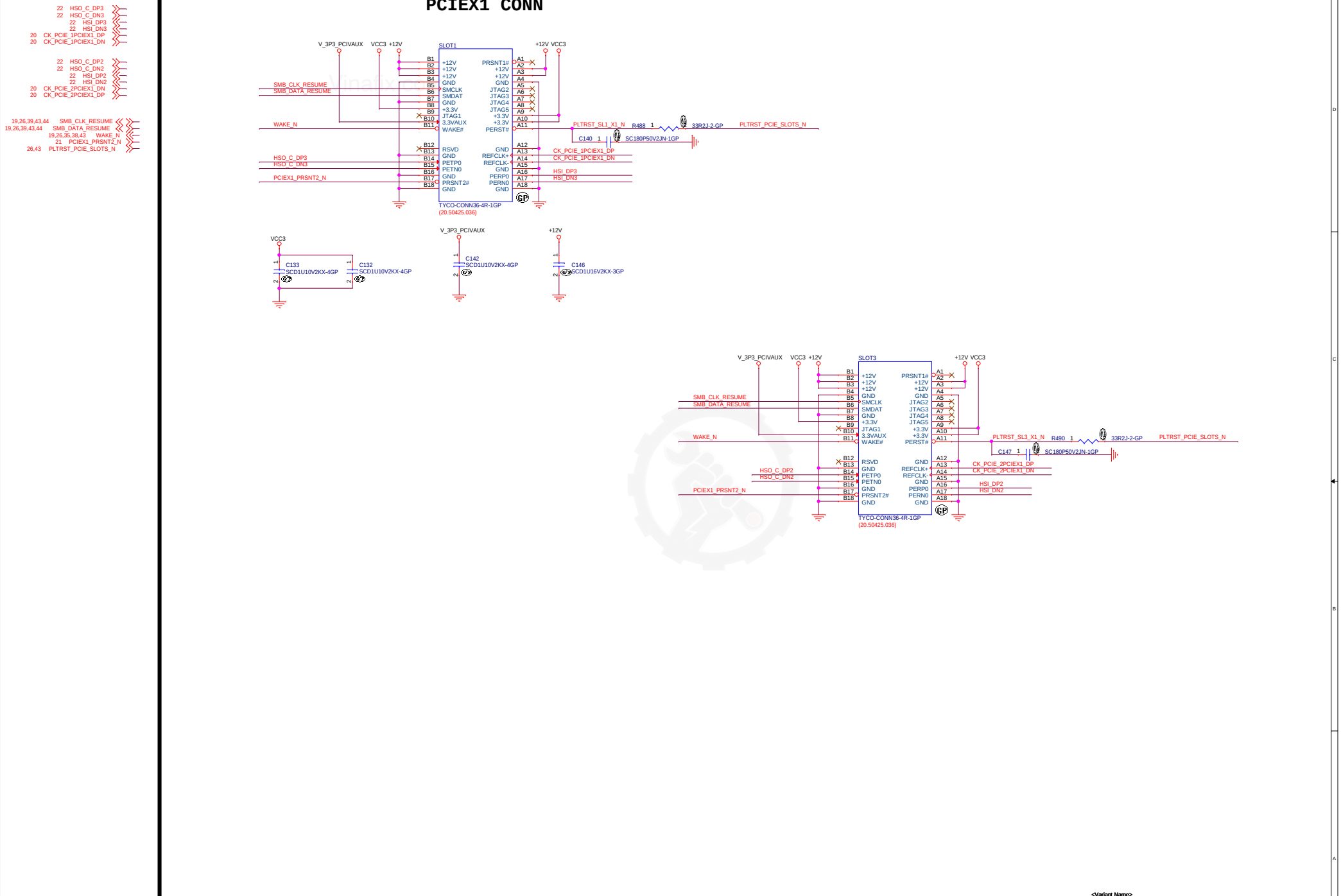
Title

TPM

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 41 of 52

PCIEX1 CONN



<Variant Name>

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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCIEX1 CONN

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Monday, August 05, 2013 Sheet 42 of 52

Wireless Card(Present support EP/SP)

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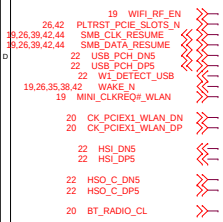
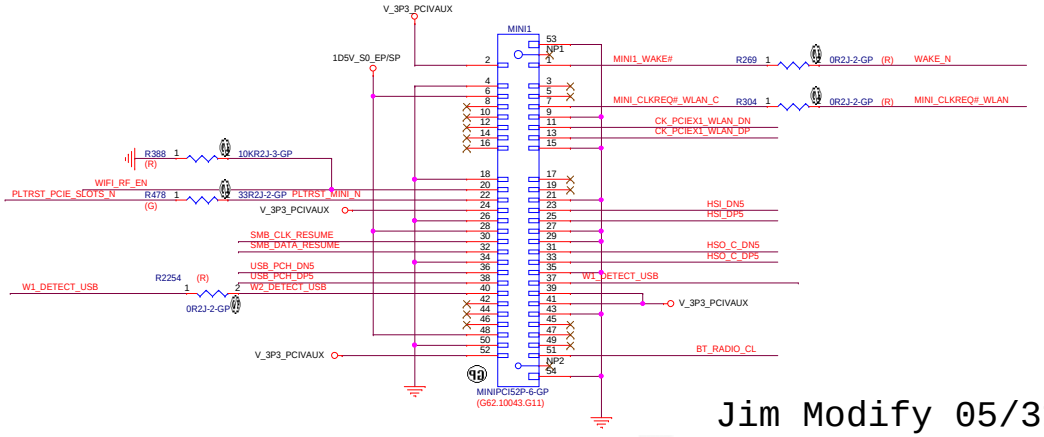
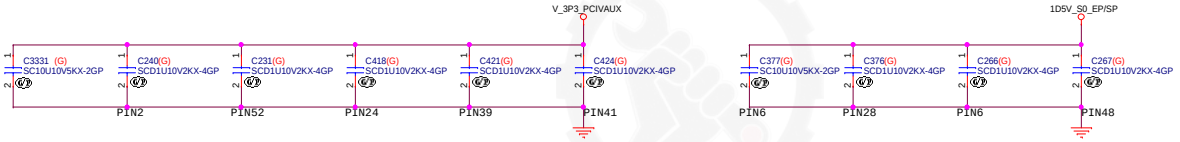
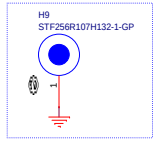
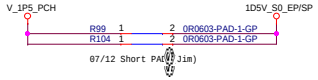




Jim Modify 05/31







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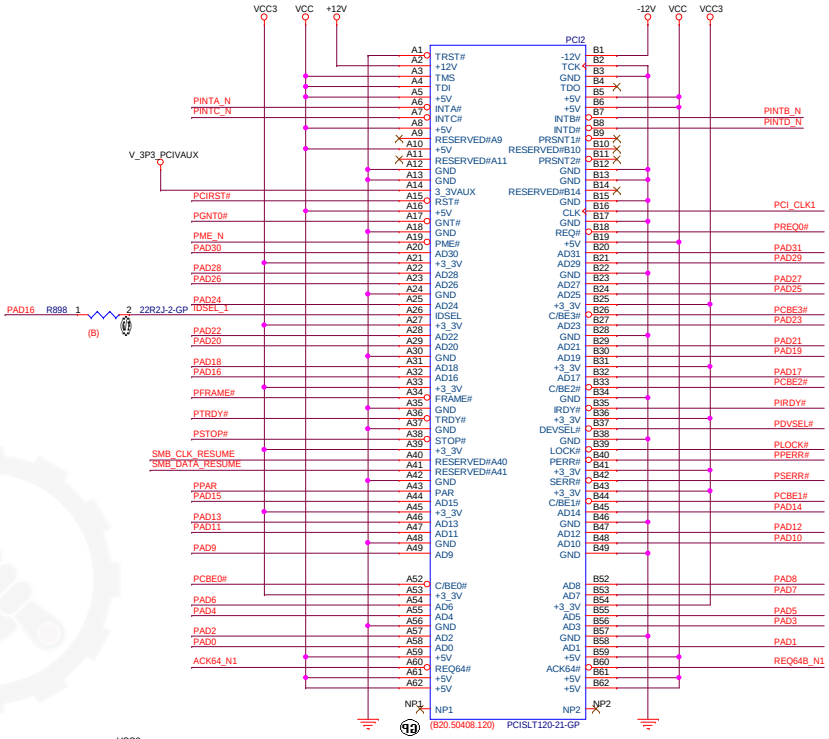
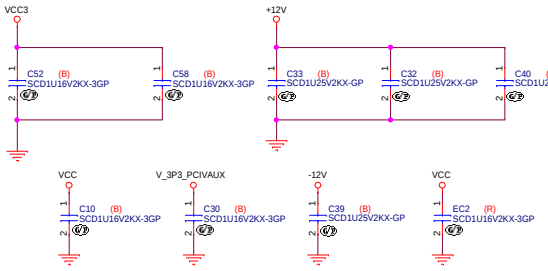
wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: MINI PCIC SLOT		
Size: C	Document Number: ROSA Shark Bay DTX	Rev: SA
Date: Wednesday, August 28, 2013	Sheet 43 of 52	

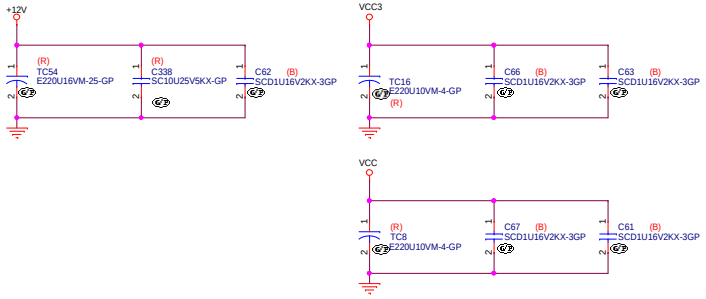
Vinafix.com

38 PCI_CLK1
38 PCIRST#
38 PGNT0#
38 PREQ0#
38 PAD[31:0]
38 PFRAME#
38 PIRDY#
38 PTRDY#
38 PSTOP#
38 PDVSEL#
38 PINTA_N
38 PINTB_N
38 PINTC_N
38 PINTD_N
38 PLOCK#
38 PPAR
38 PPERR#
38 PSERR#
38 PME_N
38 PCBE0#
38 PCBE1#
38 PCBE2#
38 PCBE3#
19,26,39,42,43 SMB_CLK_RESUME
19,26,39,42,43 SMB_DATA_RESUME



Decoupling Cap





Place Near PCI Slot

<Variant Name>

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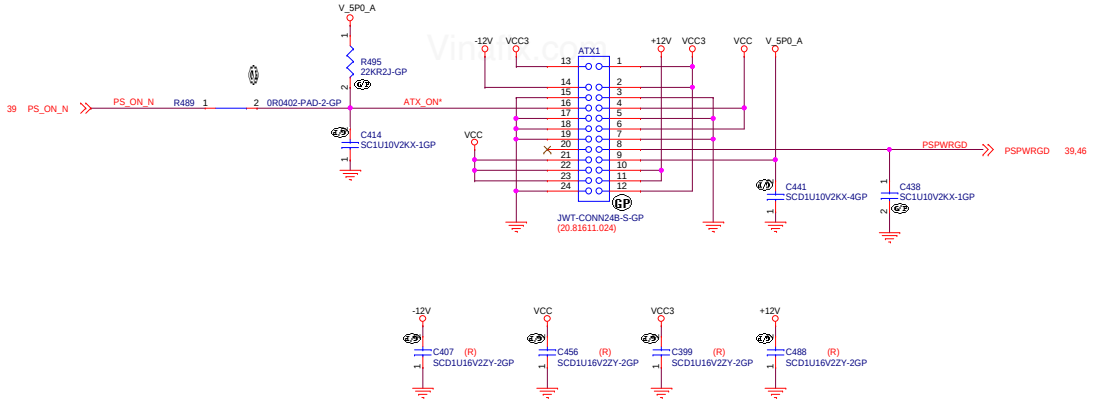
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCI SLOT

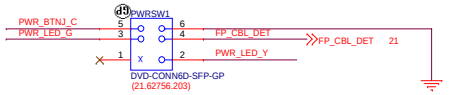
Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 44 of 52

ATX CONNECTOR

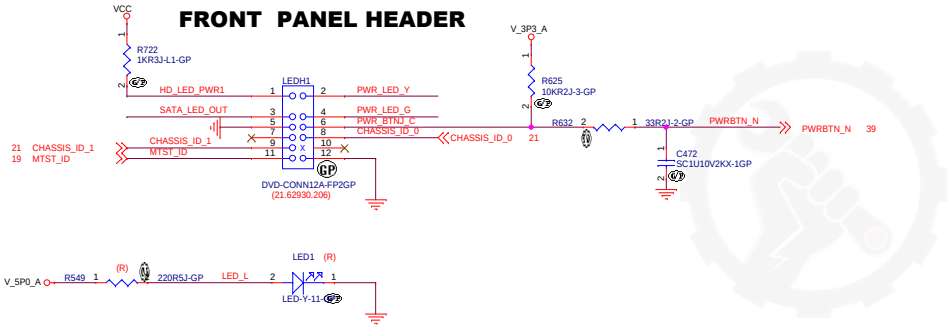


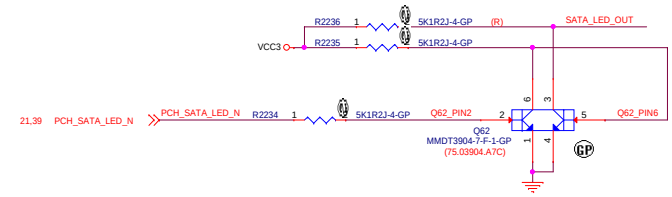
POWER BUTTON



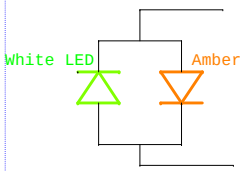
Jim Modify 0617

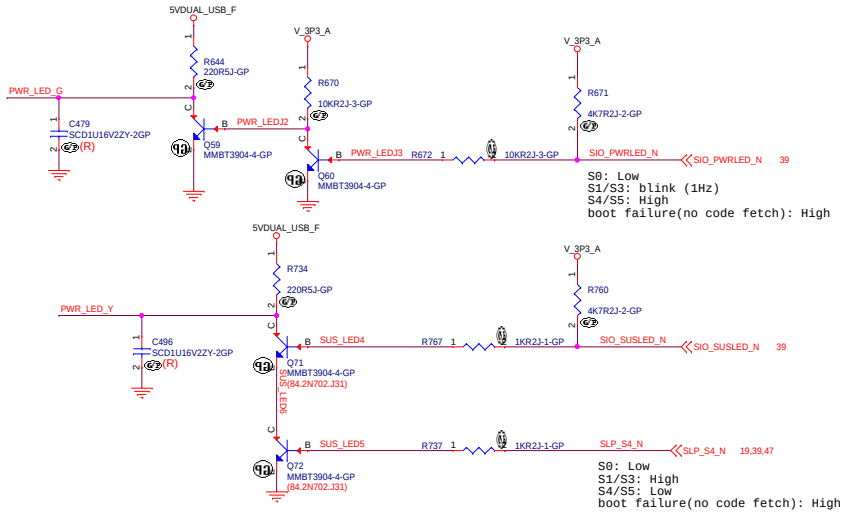
FRONT PANEL HEADER





S0	White
S3	Amber
S4	LED off
No Post	Amber
Failure to Post	Amber (blinking)





<Variant Name>

wistron

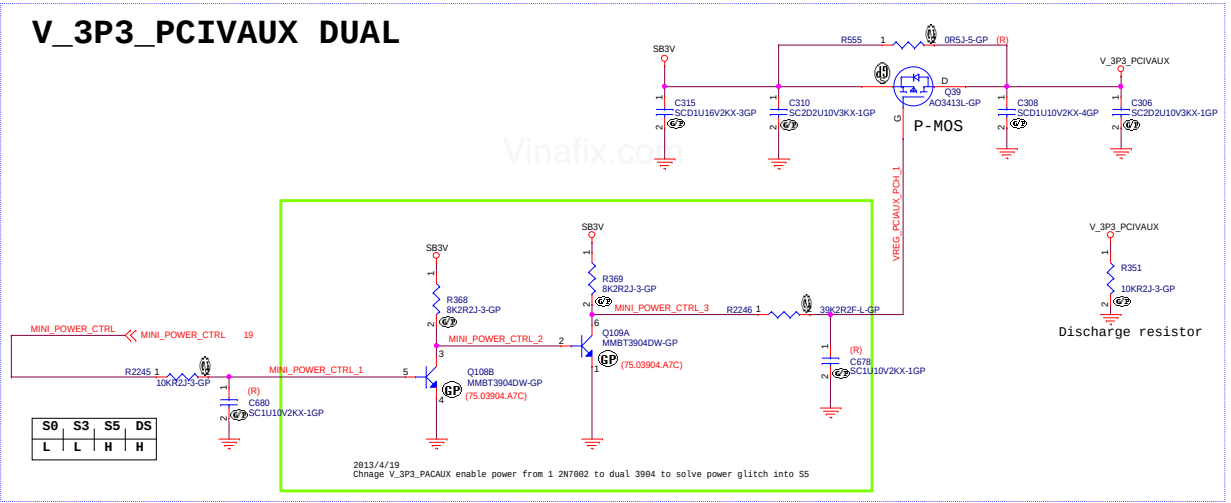
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PWR/FNT PNL

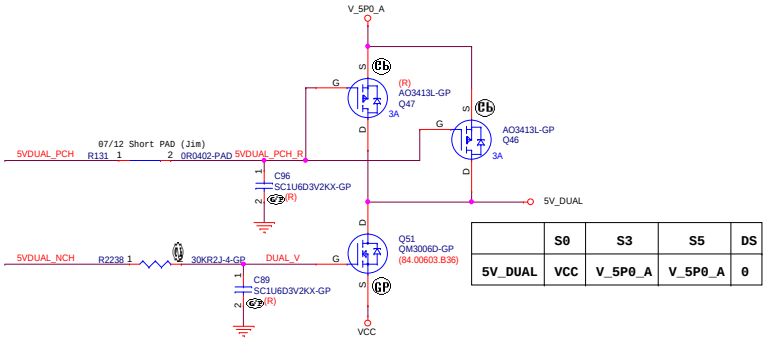
Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Monday, August 05, 2013 | Sheet 45 of 52

V_3P3_PCIVAUX DUAL

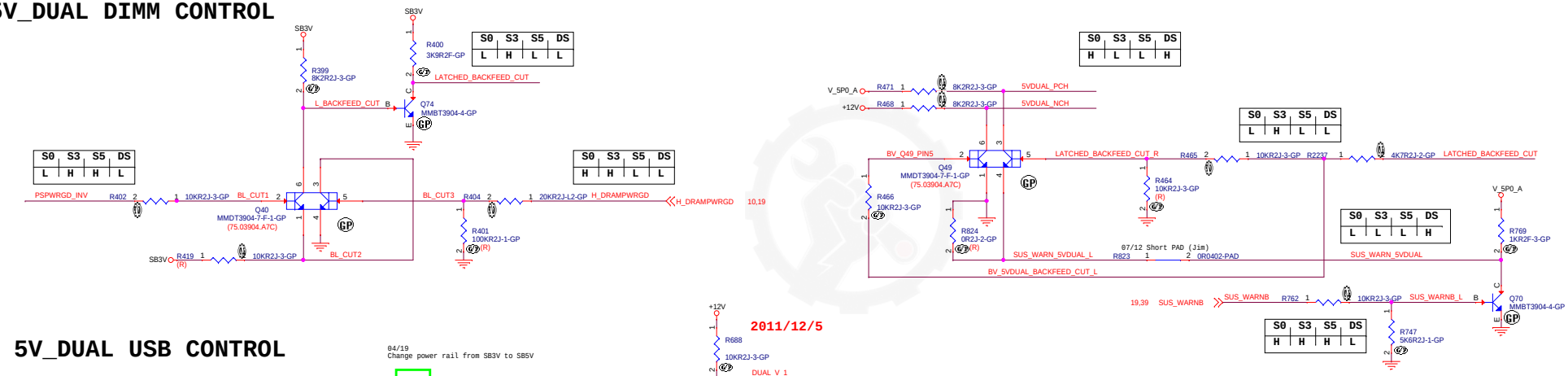


DIMM 5V_DUAL

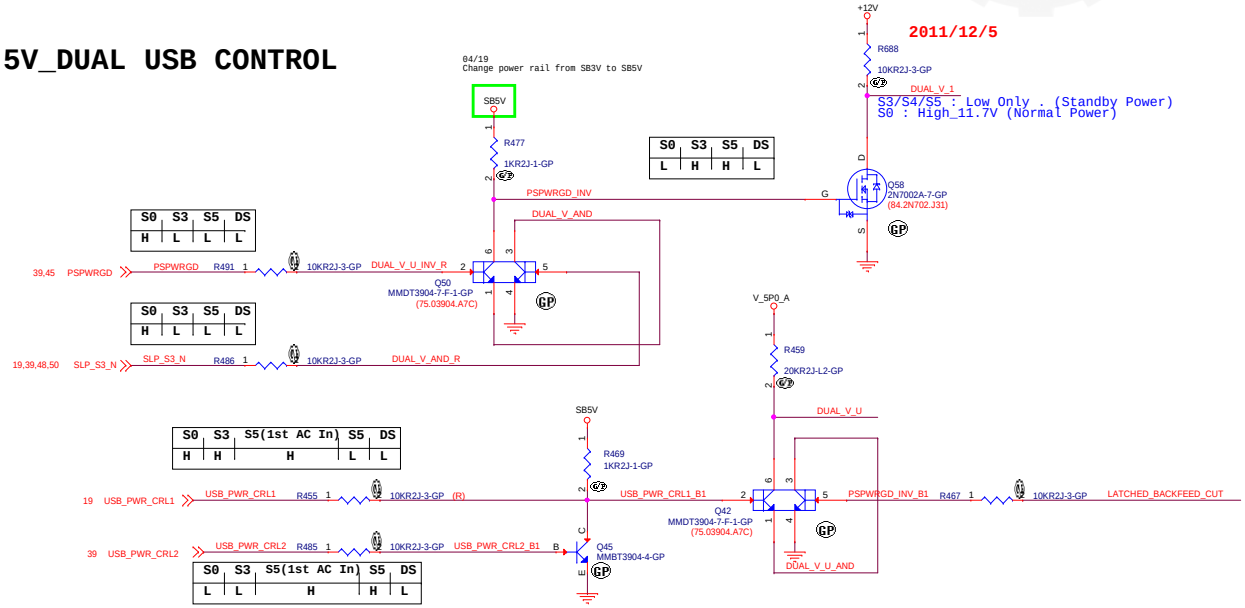


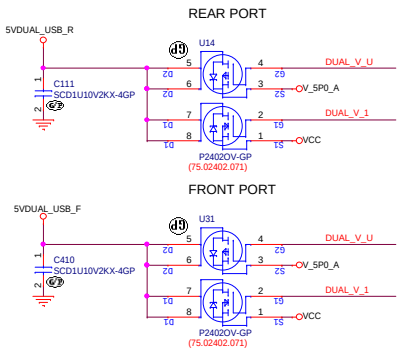
	S0	S3	S5	DS
5V_DUAL	VCC	V_5P0_A	V_5P0_A	0

5V_DUAL DIMM CONTROL



5V_DUAL USB CONTROL





	S0	S3	S5	DS
5VDUAL_USB_R	VCC	SB5V	0	0
5VDUAL_USB_F	VCC	SB5V	0	0

<Variant Name>

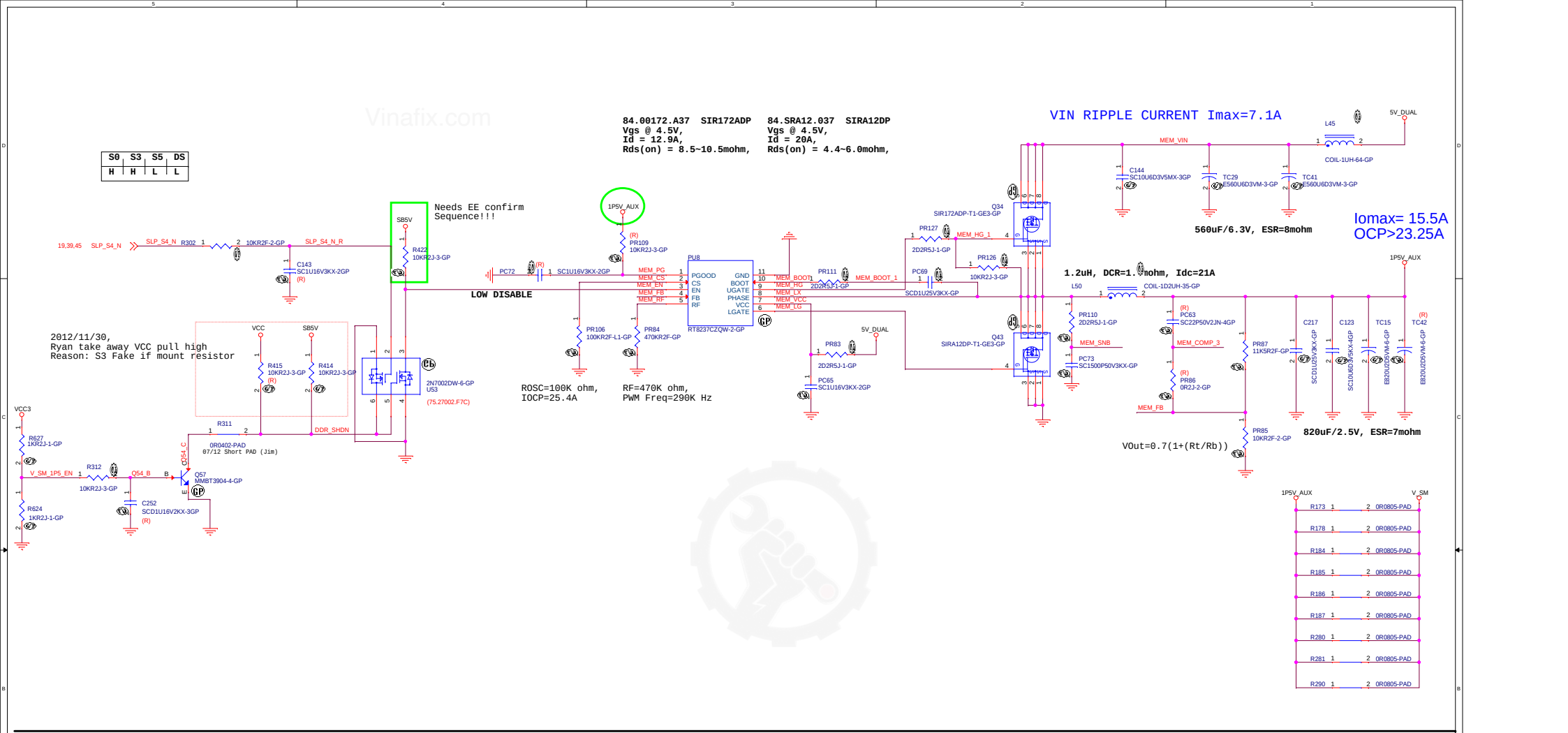
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DUAL POWER

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 46 of 52


S0 S3 S5 DS
H H L L
84.00172.A37 SIR172ADP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 8.5~10.5mohm,
84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,
VIN RIPPLE CURRENT Imax=7.1A
Needs EE confirm Sequence!!!
LOW DISABLE
2012/11/30,
Ryan take away VCC pull high
Reason: S3 Fake if mount resistor
ROSC=100K ohm,
IOCP=25.4A
RF=470K ohm,
PWM Freq=290K Hz
1.2uH, DCR=1.0mohm, Idc=21A
Iomax= 15.5A
OCP>23.25A
560uF/6.3V, ESR=8mohm
820uF/2.5V, ESR=7mohm
VOut=0.7(1+(Rt/Rb))
DDR3 MEM_VTT
(0.75V)
Iomax=1A
2013/4/2
Delete reserve TC46

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<Variant Name>
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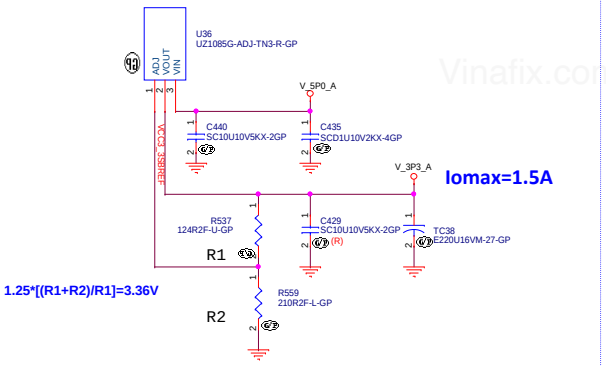
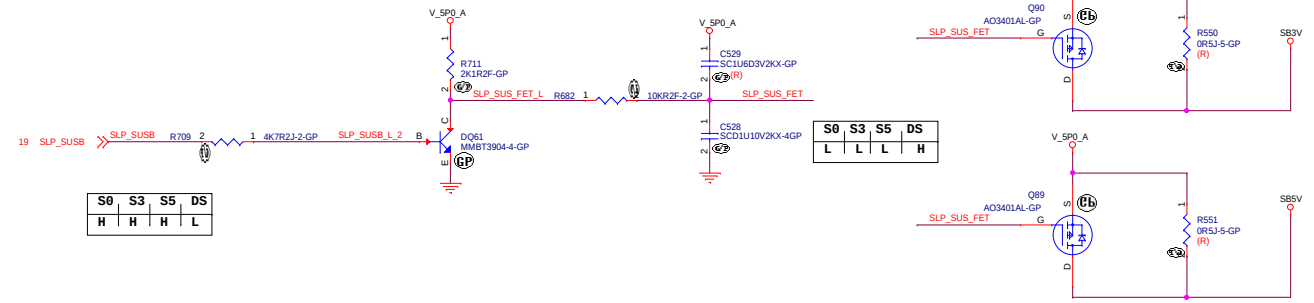
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
DDR POWER
Size C
Document Number ROSA Shark Bay DTX
Rev SA
Date: Tuesday, August 06, 2013
Sheet 47 of 52

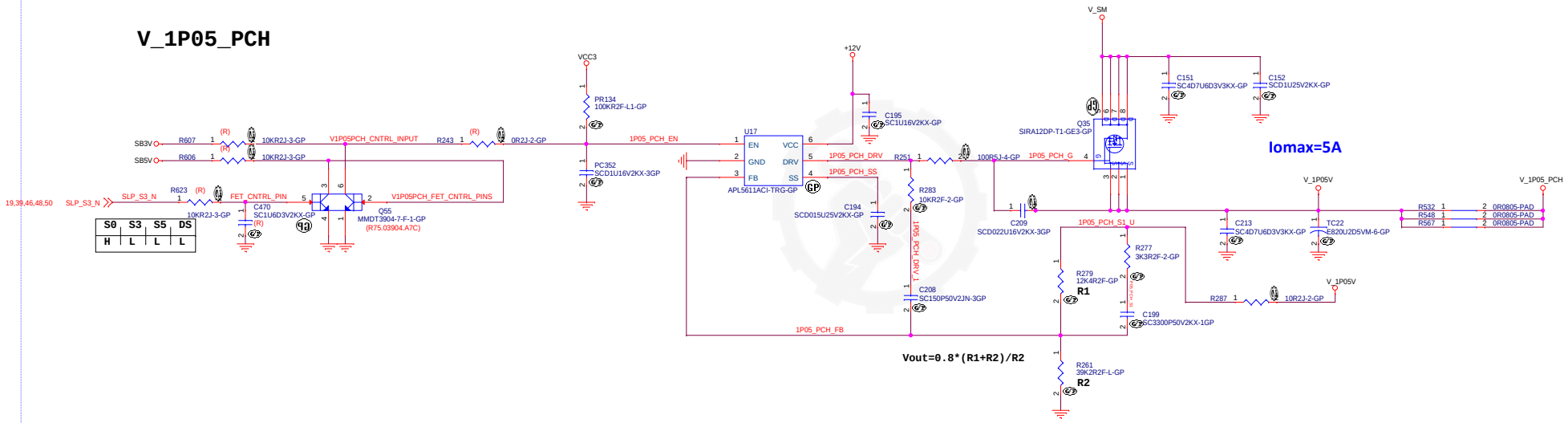
V_3P3_A 1.5A



SB5V/SB3V

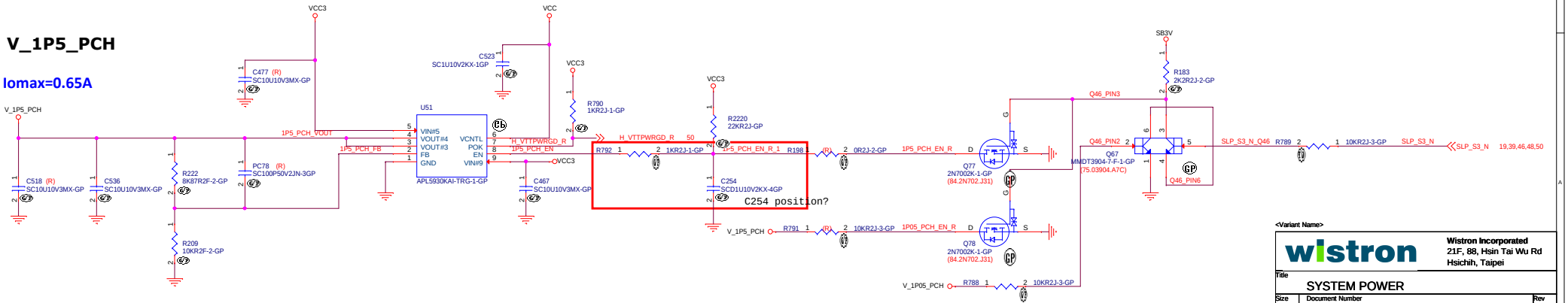


V_1P05_PCH



V_1P5_PCH

Iomax=0.65A



<variant_name>

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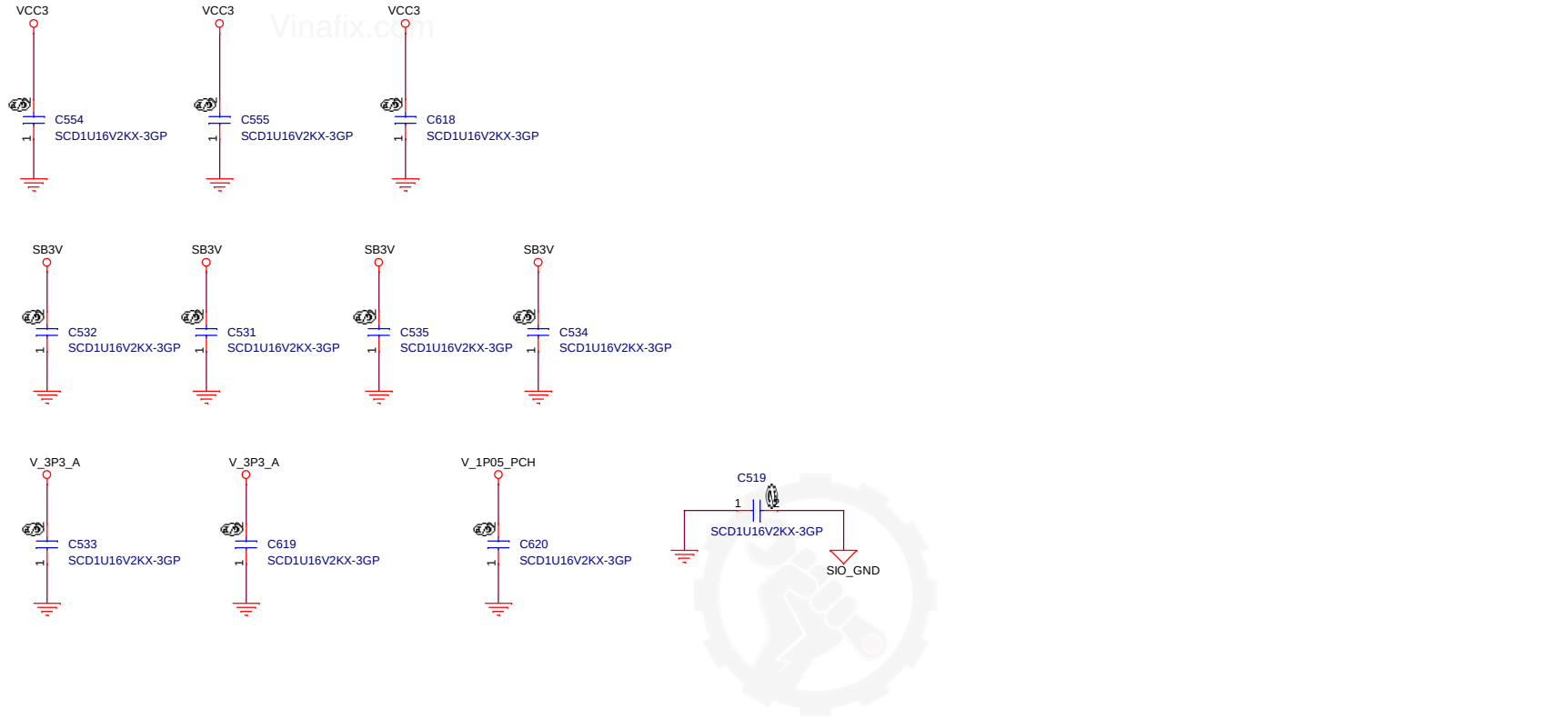
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SYSTEM POWER

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 48 of 52



<Variant Name>

wistron

Wistron Incorporated
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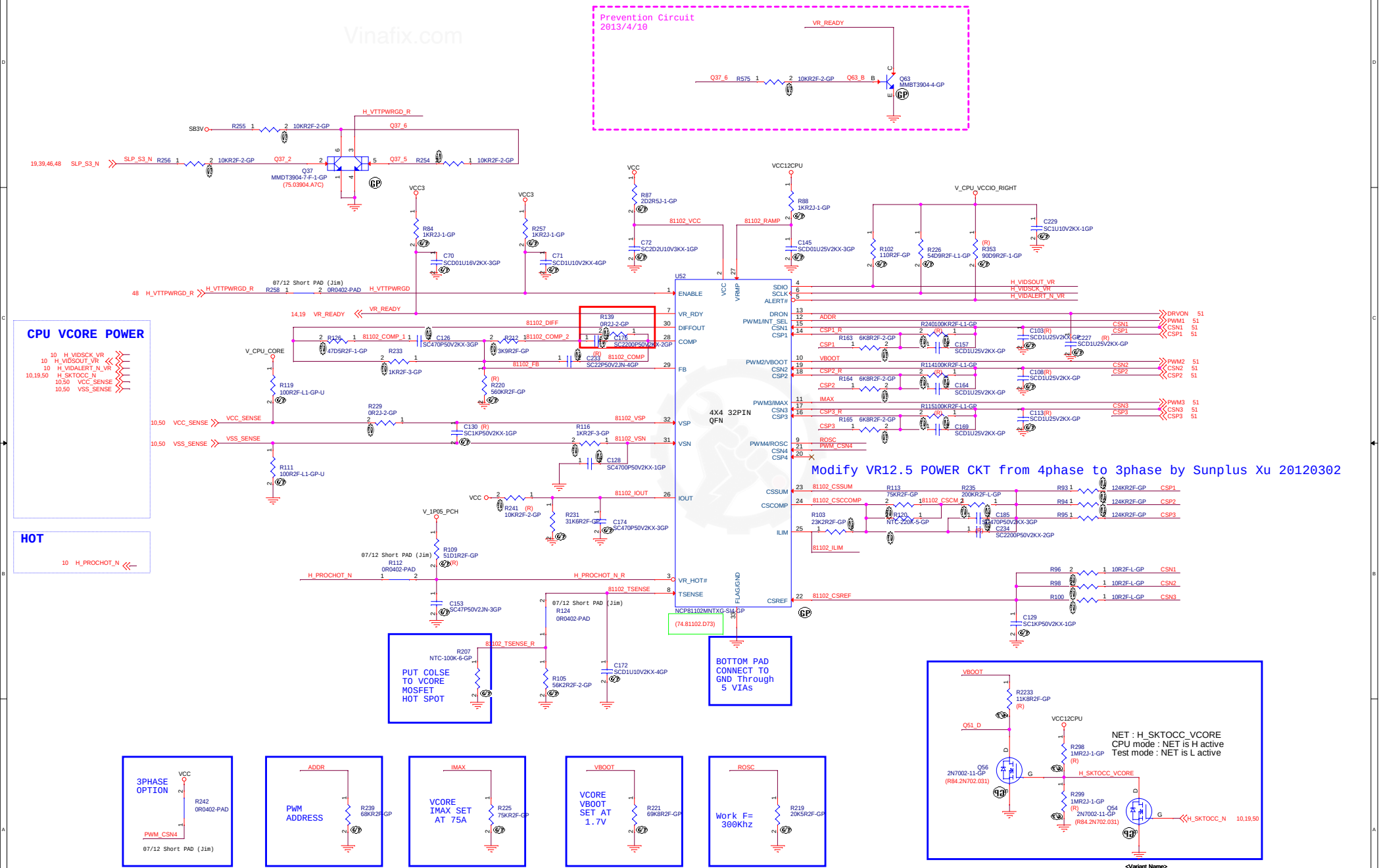
Title: ME POWER		
Size: B	Document Number: ROSA Shark Bay DTX	Rev: SA
Date: Thursday, August 01, 2013	Sheet 49 of 52	

SharkBay VR12.5 POWER CKT - 3 PHASE



wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU_VRD 12-5_1

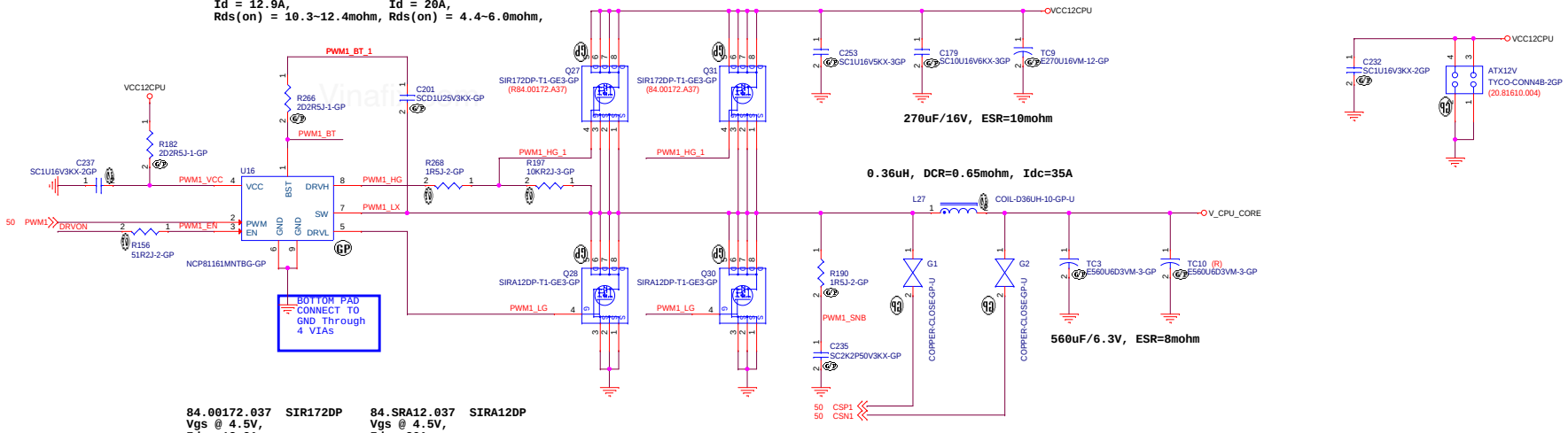
Size: C | Document Number: ROSA Shark Bay DTX | Rev: SA

Date: Thursday, August 01, 2013 | Sheet 50 of 52

84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,

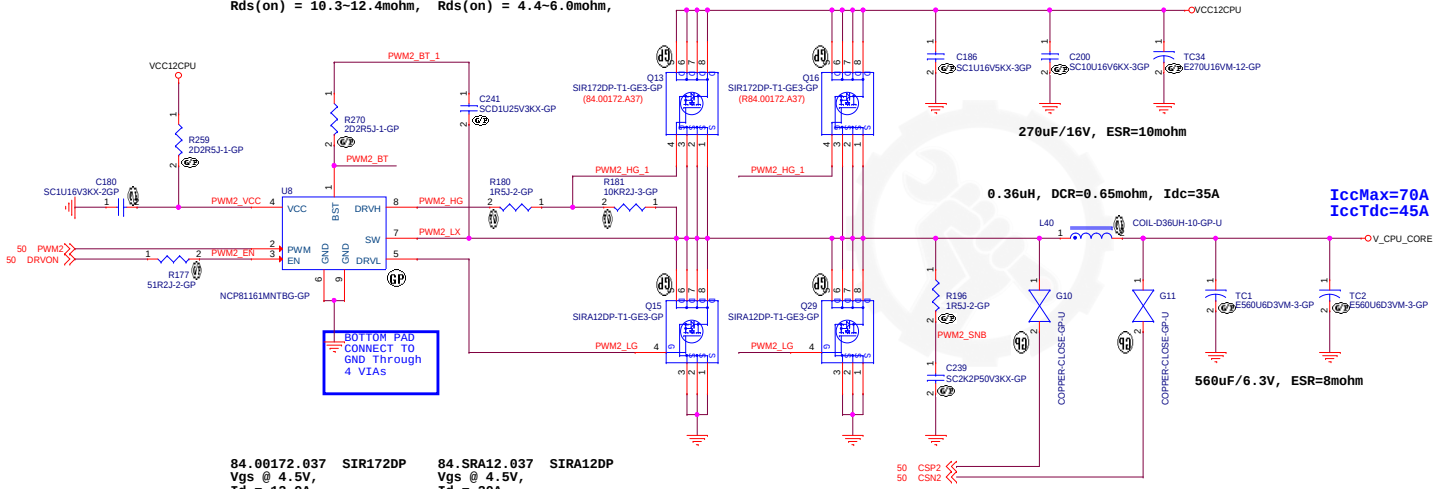
84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,

VIN RIPPLE CURRENT Imax=7.42A



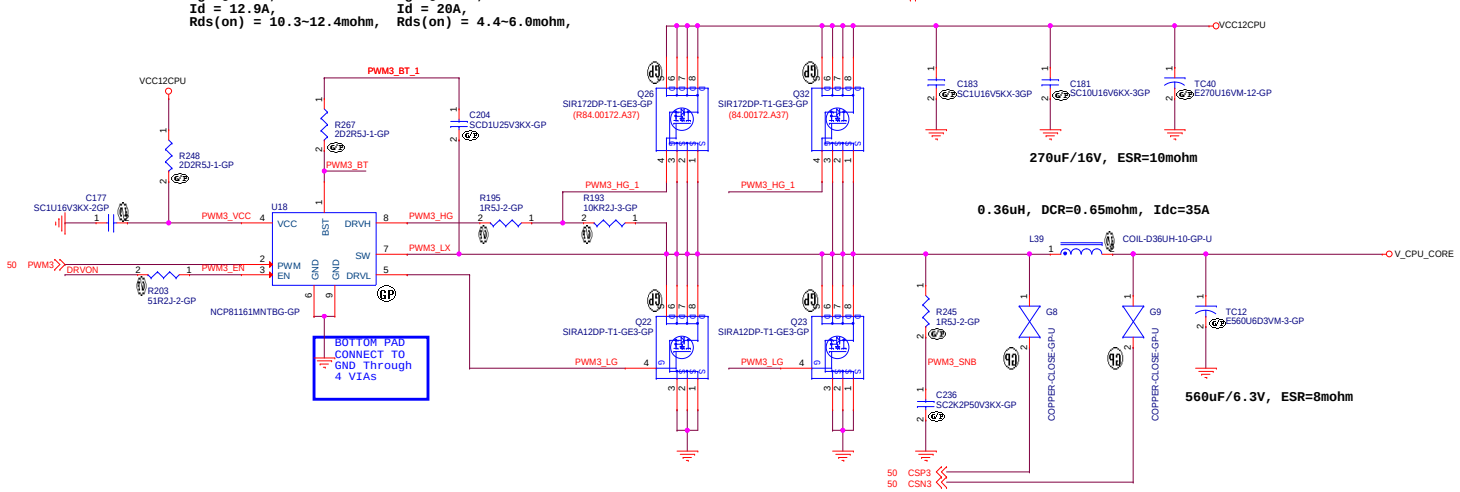
84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,



84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	CPU_VRD 12-5_2	
Size C	Document Number ROSA Shark Bay DTX	Rev SA
Date: Thursday, August 01, 2013	Sheet 51 of 52	

X00 ----> X01

1. Add Pull high 10K resister R621 for USB0C_2.3 (GB)
2. 82.30001.861 change to 82.30001.A41 for X3 32.768 Crystal Pacage
3. 09.2771D.E4L change to 09.2771D.B5L for TC34 TC40 TC9 2.5 change 3.5 pitch
4. 69.80021.001 change to 75.05125.07D for Audio ESD
5. 83.01045.AA0 change to 75.09904.07C for U6 U9 U11 LAN ESD
6. R754 change 1k for PWROK 3V
7. Add Audio Beep function
8. Remove L23 for LAN 1.05V
9. Remove TPM Function Page.41 06/17
10. Add Power button 6 Pin header in Page45 06/17
11. Add L9 for de POP Noise
12. Add R705 for LAN Drop

X01 ----> X02

1. Short PAD (FL5,L17,L20,L5,L6,L7,R2244,L4,R622,R112,R124,R258,R311,R391,R533,R561,R702,R708,
R761,R806,R131,R242,R823,,R847,R99,R104,R1215
R1216,R759,

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Change list

Size	Document Number	Rev
C	ROSA Shark Bay DTX	SA

Date: Thursday, August 01, 2013 Sheet 52 of 52